

## ***22A PROM PROGRAMMER***

10-990-0003 REV H  
Applies to configuration 990-0003-007

APR 84

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## SECTION 1

# INTRODUCTION

### 1.1 GENERAL INFORMATION

The 22A is Data I/O's fully integrated portable programmer. It is capable of programming many different kinds of PROMs. For a list of specific devices that the 22A programs, refer to the information in table 1-1. Most MOS PROMs can be programmed by using the fixed 28-pin socket located to the right of the 22A's keyboard. Other devices may require the use of additional socket adapters listed in table 1-1.

In addition to the programming convenience of programming many devices in a single package, the 22A contains a built-in ultra violet (UV) lamp for erasing MOS devices.

The 22A utilizes a full hexadecimal keypad and a 16-character alphanumeric florescent display to provide data entry and editing from the front panel. A standard 32K byte x 8 data RAM gives you the flexibility to handle large amounts of data. A serial I/O port is also standard. The RS232 port provides the ability to interface to different kinds of peripheral equipment for data transfers and remote control operations.

#### 1.1.1 THE 22A APPROACH TO PROGRAMMING

Values for programming variables, including pinouts, voltage levels and timing are stored in firmware tables within the 22A. When you choose the family and pinout codes for a particular device, the programmer uses the information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead.

To maximize control speed during programming, the 22A makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

### 1.2 THEORY OF OPERATION

The 22A is easy to operate. As you can see from figure 1-1, each of the four major operations of the 22A has its own key (blue) assignment on the front panel keyboard. Each of these mode keys and their uses are discussed in the following subsections.

Operations performed by the 22A consist of:

- Copy—moves data from a source (device, RAM or Port) to a destination (device, RAM or Port).
- Verify—compares data between a source and destination.

#### NOTE

*Both Copy and Verify operations follow the source/destination method of data transfer and verification. In short, the operator initiates the operation by choosing either the COPY or VERIFY key and then specifies the source of data (device, RAM or port) and then the destination for that data (again, either device, RAM or port). This concept is explained in detail in section 3.7.*

- Edit—changes data at selected addresses within the programmer RAM.
- Select Function—allows you to either manipulate RAM data or change various operating parameters.

Section 3 of this manual (Operation) provides specific step-by-step instructions on how to execute the operations listed in the following subsections.

#### 1.2.1 THE COPY KEY

The COPY key is used to copy data from one medium to another or one RAM location to another. When the COPY key is used, data is moved from the source to the destination; for example, from the programmer data RAM to a blank device in the socket. At the completion of this operation the device will contain a copy of the data in the programmer data RAM - the device is now "programmed". The "source/destination" concept is explained in section 3.7.

There are five basic types of copy operations. Instructions for performing the specific bulleted operations which follow, are located in section 3.

1. A data transfer from a device to the programmer RAM is a Load operation.
  - Load with Master Device Data
2. A data transfer from the serial port to the programmer RAM is an Input operation.
  - Input from Port
3. A data transfer from the programmer RAM to a device is a Program operation.
  - Program Device

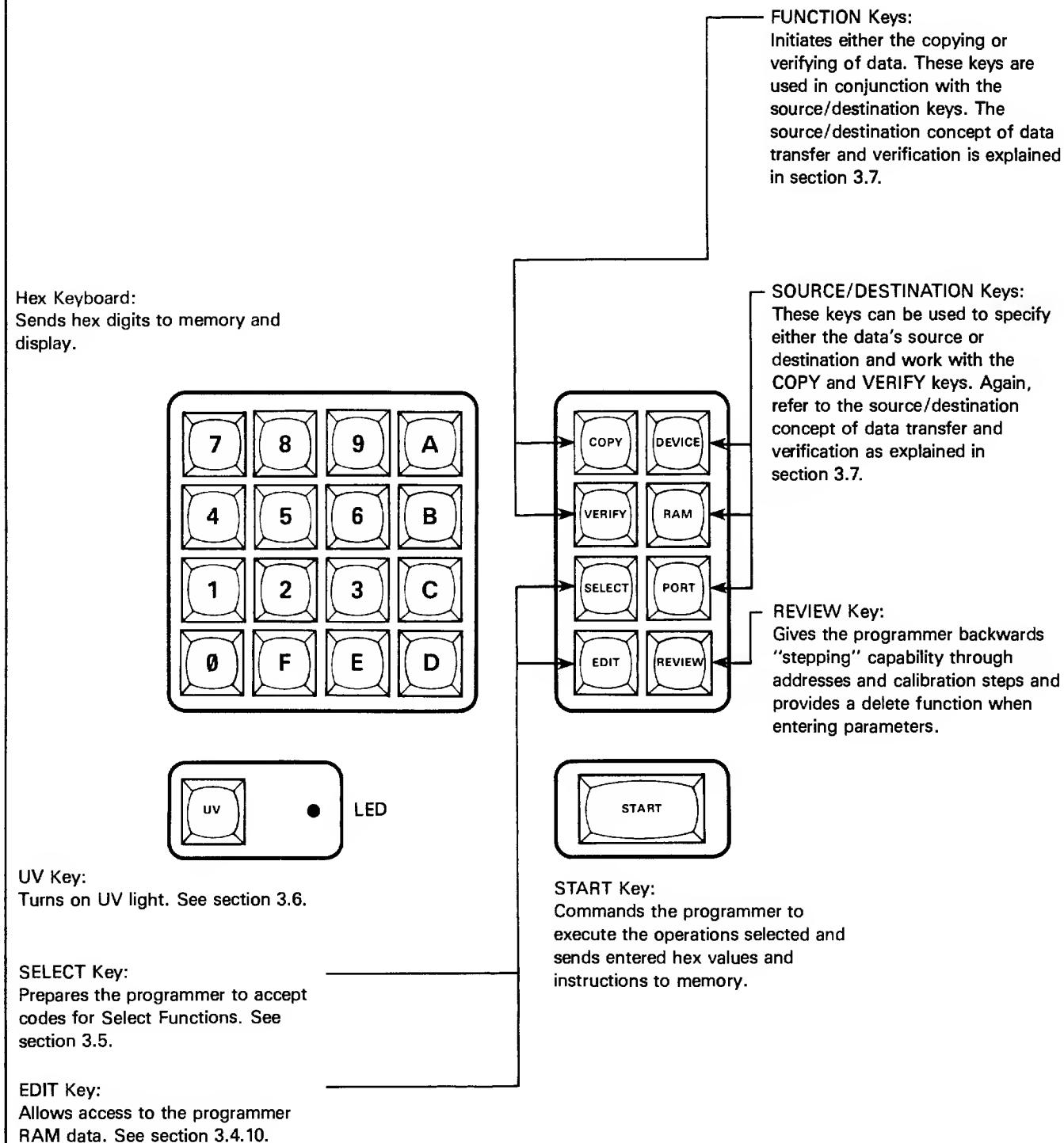


Figure 1-1. Tasks Performed by the Keys on the 22A Keyboard

4. A data transfer from the programmer RAM to the serial port is an **Output** operation.
  - Output to Port
5. A data transfer that moves a block of RAM data to another location within RAM is a **Block Move**.
  - Block Move

**LOAD.** A load operation consists of taking programming data from a master device and transferring it to the programmer RAM. When the data transfer is complete, the 22A calculates the sum-check (see Glossary for definition) of the loaded data and displays it.

**INPUT.** In an input operation, data received at the serial port is translated and transferred to the programmer RAM. When completed, the programmer calculates and displays the sum-check of the data. If a sum-check has been sent with the data from the serial port, the programmer will compare the two and signal an error if they do not match.

**PROGRAM.** A program operation duplicates the data in the programmer RAM into a device. Programming is automatic starting with an illegal bit test and a blank check (see Glossary for definition) to insure that the device can be programmed. Data is then programmed into the device in the socket one byte at a time. This continues until all data bytes have been programmed into the device. After programming is completed, the data in the device is automatically compared with the source data to insure correct programming.

**OUTPUT.** In an output operation, data from the programmer RAM is translated and transferred to the serial port.

**BLOCK MOVE.** A Block move is accomplished by using the COPY key. In a Block Move, blocks of data within RAM can be rearranged. Refer to figure 1-2.

### 1.2.2 THE VERIFY KEY

The VERIFY key is used to make a byte-by-byte comparison of data in two locations, one referred to as the "source" and one as the "destination". The source/destination method of syntax is explained in section 3-7.

There are two types of Verify operations. Instructions for performing the bulleted operations are located in Section 3.

1. **Verify Device.** In a verify device operation, data from the device (the destination) is compared byte-by-byte twice with the data in RAM (the source). On the first pass (first comparison), parametric checking is done by lowering VCC within the manufacturer's specified lower level. On the second pass, VCC is raised to the upper level specification range.
  - Verify Device
2. **Input Verify.** In an input verify operation, incoming data from the serial port is compared byte-by-byte with the data in RAM.
  - Input Verify

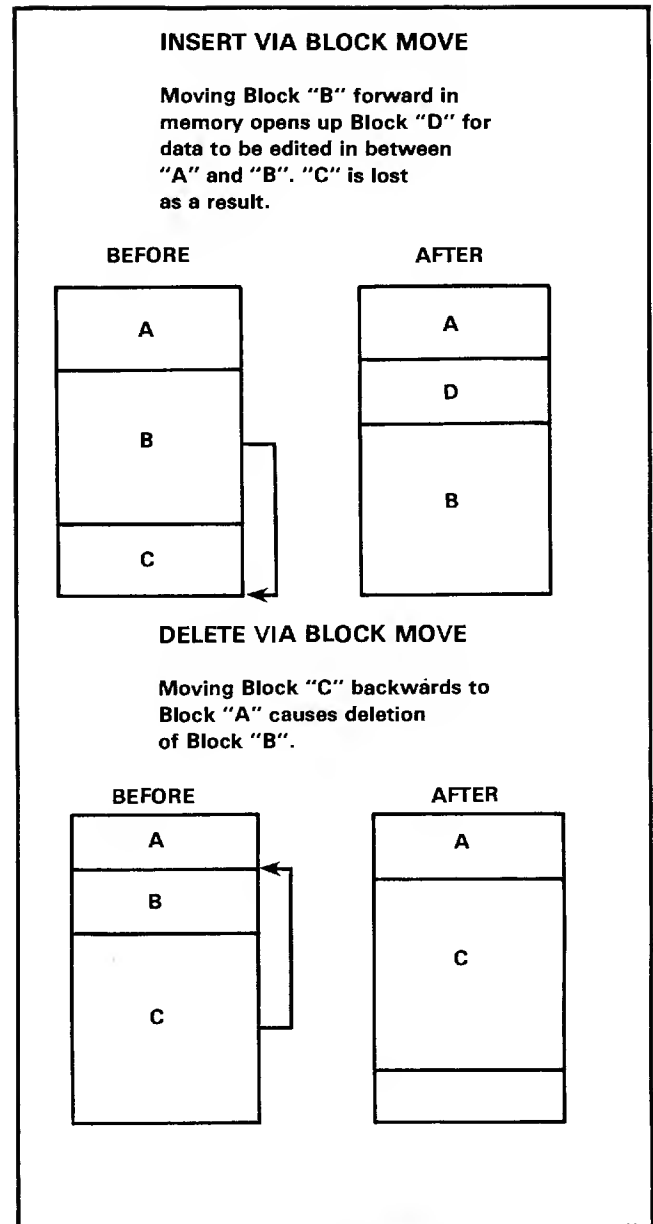


Figure 1-2. Block Move

### 1.2.3 THE EDIT KEY

The EDIT key allows you to view and change data at specified RAM addresses. Section 3 provides specific details.

### 1.2.4 THE SELECT KEY

The SELECT key allows you to change certain operational parameter default values, perform RAM data manipulations and access certain less frequently used operations. These operations are referred to in this manual as Select Functions. Detailed Select Function information and operation is located in section 3.5.

### 1.3 HOW TO USE THIS MANUAL

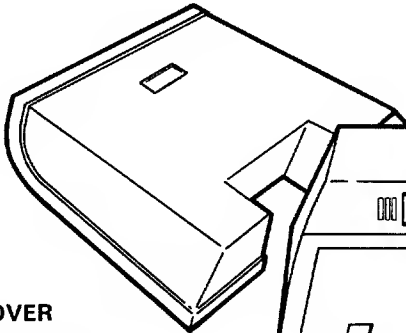
Using the 22A programmer is easy. Figure 1-3 illustrates the programming components of the 22A. The illustration explains how to set these components up so you can start programming right away. It is a central reference point directing you to specific locations within the manual.

### 1.4 SPECIFICATIONS

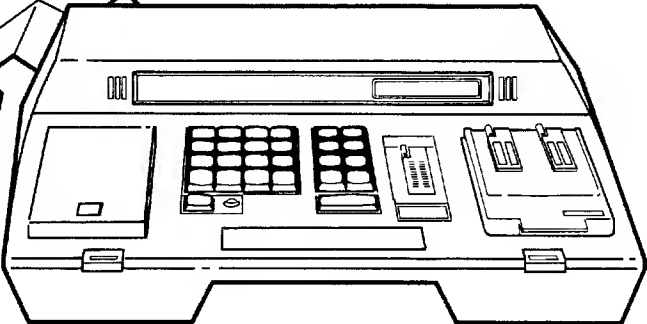
The following subsections describe the major components and power requirements of your programmer.


<u>Situation</u>	<u>Reference Point</u>	<u>Situation</u>	<u>Reference Point</u>
1. Plugging in your programmer and applying power	Consult Section 2.4.4	4. If, according to table 1-1, a special socket adapter is required to program this device...	Read section 2.5 for installation instructions
2. Serial I/O Operation Yes No	Read Section 2.6 Continue to next step	5. Select your programming operation.	Read section 3.1
3. Select the device you wish to program, and its corresponding family and pinout code, from table 1-1.		6. Execute the operation.	Consult section 3.4
		7. Data manipulation required?	Refer to section 3.5
		8. Remote Control operation?	Read section 3.8

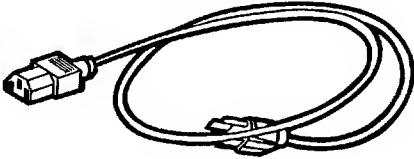


**DUST COVER**  
Instructions for installing or removing your dust cover are located in section 2.2.

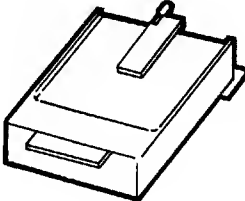




**OPERATOR GUIDE**  
The Operator Guide is located inside the dust cover. It contains reference information for commonly used operations.



**POWER CORD**  
Instructions for plugging in your programmer and applying power are located in section 2.4.4.



**OPTIONAL SOCKET ADAPTER**  
Instructions for installing or removing a socket adapter are located in section 2.5.

Figure 1-3. Using the 22A Manual to Meet Your Programming Needs

### 1.4.1 MAJOR COMPONENTS

The 22A is a self-contained portable programmer. This unit has a 32K x 8 data RAM.

The unit's serial I/O port can be used to accept or transmit data from a peripheral device, or allow for remote control operations.

Since all programming electronics reside within the programmer, there is no need for extra programming modules; however, certain devices do require a socket adapter for programming. Most MOS PROMs can be programmed by using the fixed 28-pin socket located on the programmer's front panel. Table 1-1 provides a quick reference to the socket (or socket adapter) you need to use to program your device.

Voltages are current limited and regulated to meet the device manufacturers' programming specifications.

### 1.4.2 POWER REQUIREMENTS

The following are the 22A's power requirements. Section 2.3 discusses power connection.

- Operating Voltages: 100, 120, 220, 240 VAC ( $\pm 10\%$ )
- Frequency Range: 48 - 62 Hz
- Input Power: minimum 28 watts  
maximum 72 watts

The 22A's physical and environmental specifications are listed below:

- |                               |   |
|-------------------------------|---|
| • Dimensions                  | 34 x 43 x 11 cm<br>(13.5" x 17" x 4.5") |
| • Weight                      | 16 lbs.                                 |
| • Operating Temperature Range | 5° to 45°<br>(41° to 113°F)             |
| • Storage Temperature Range   | -40° to 70°<br>(-40° to 158°F)          |
| • Relative Humidity           | 90% noncondensing                       |

### 1.4.3 DATA TRANSLATION FORMATS

Appendix A provides specific details for each data translation format available on the 22A.

## 1.5 FIELD APPLICATIONS SUPPORT

Data I/O has Field Applications Engineers (FAEs) who can provide you additional information about interfacing Data I/O products with other equipment or answer your questions about problems you may have with your equipment.

The location of the FAE nearest you is given on the address list at the back of this manual. Call your FAE if you have any questions or problems.

## 1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period is one year and begins when you receive the programmer. The warranty card at the back of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

## 1.7 SERVICE

Data I/O maintains Service Centers throughout the world, each staffed with factory trained technicians to provide prompt, quality service. A list of all the Service Centers is located at the back of this manual.

## 1.8 ORDERING

To place an order for equipment, contact your Data I/O Sales Representative.

Orders for shipment must include the following:

- description of the equipment; see the latest Data I/O Price list or contact your sales representative for equipment and part numbers,
- purchase order number,
- desired method of shipment,
- quantity of each item ordered,
- shipping and billing address of firm, including zip code, and
- name of person ordering the equipment.



Table 1-1. Family and Pinout Codes

Device Part Number	Family and Pinout Code	Software Version	Adapter	Approval Status	Device Part Number	Family and Pinout Code	Software Version	Adapter	Approval Status		
Advanced Micro Devices					Advencad Micro Devices (Cont.)						
27LS18	16	02	V01	351A-064	S	27S49	16	67	V01	-	S
27LS19	16	02	V01	351A-064	S						
27S08	15	02	V01	351A-064	O	2708	21	27	V01	-	A
27S09	15	02	V01	351A-064	O	AM9708	21	27	V01	-	A
					2716	19	23	V01	-	A	
27S18	16	02	V01	351A-064	A	AM9716	19	23	V01	-	A
27S19	16	02	V01	351A-064	A						
29750A	16	02	V01	351A-064	A	2732	19	24	V01	-	A
29751A	16	02	V01	351A-064	A	2732A	27	24	V01	-	A
					AM9732	19	24	V01	-	A	
27S10	15	01	V01	351A-064	O	2764	AF	33	V01	-	A
27S11	15	01	V01	351A-064	O						
27S20	16	01	V01	351A-064	A	AM9764	AF	33	V01	-	A
27S21	16	01	V01	351A-064	A	27128	AF	51	V01	-	A
					Electronic Arrays						
29760A	16	01	V01	351A-064	A	2708	21	27	V01	-	O
29761A	16	01	V01	351A-064	A	2716	19	23	V01	-	O
27S12	16	03	V01	351A-064	A						
27S13	16	03	V01	351A-064	A	Feirchild					
					93417	01	01	V01	351A-064	A	
29770	16	03	V01	351A-064	A	93427	01	01	V01	351A-064	A
29771	16	03	V01	351A-064	A	93436	01	03	V01	351A-064	A
27S24	16	65	V01	351A-074	S	93446	01	03	V01	351A-064	A
27S25	16	65	V01	351A-074	S						
					93438	01	15	V01	-	A	
27S28	16	09	V01	351A-064	A	93448	01	15	V01	-	A
27S29	16	09	V01	351A-064	A	93452	01	05	V01	351A-064	A
27S30	16	36	V01	-	A	93453	01	05	V01	351A-064	A
27S31	16	36	V01	-	A						
					93450	01	16	V01	-	A	
27S32	16	38	V01	351A-064	A	93451	01	16	V01	-	A
27S33	16	38	V01	351A-064	A	93460	01	16	V01	-	S
27PS181	16	37	V01	-	S	93461	01	16	V01	-	S
27PS281	16	37	V01	351A-074	S						
					93L450	01	16	V01	-	S	
27S180	16	37	V01	-	A	93L451	01	16	V01	-	S
27S181	16	37	V01	-	A	93514	01	06	V01	351A-064	S
27S280	16	37	V01	351A-074	S	93515	01	06	V01	351A-064	S
27S281	16	37	V01	351A-074	S						
					93510	01	21	V01	-	A	
27S35	16	66	V01	351A-074	S	93511	01	21	V01	-	A
27S37	16	66	V01	351A-074	S						
27LS185	16	06	V01	351A-064	S	2708	21	27	V01	-	S
27PS184	16	06	V01	351A-064	S	Fujitsu					
					27C32A	27	24	V01	-	S	
27PS185	16	06	V01	351A-064	A	27C64	45	33	V01	-	S
27PS184	16	06	V01	351A-064	A	7051	78	02	V01	351A-064	S
27PS191	16	68	V01	-	S	7056	78	02	V01	351A-064	S
27PS291	16	68	V01	351A-074	S	7111	68	02	V01	351A-064	S
27S190	16	68	V01	-	A	7112	68	02	V01	351A-064	S
27S191	16	68	V01	-	A	7052	78	01	V01	351A-064	S
27S290	16	68	V01	351A-074	S	7057	78	01	V01	351A-064	S
27S291	16	68	V01	351A-074	S	7113	68	01	V01	351A-064	S
27S45	16	77	V01	351A-074	S	7114	68	01	V01	351A-064	S
27S47	16	77	V01	351A-074	S	7117	68	08	V01	351A-064	S
27PS41	16	53	V01	351A-064	S	7118	68	08	V01	351A-064	S
27S40	16	53	V01	351A-064	A	7119	68	14	V01	-	S
27S41	16	53	V01	351A-064	A	7120	68	14	V01	-	S
27PS43	16	63	V01	-	A	7053	78	03	V01	351A-064	S
27S43	16	63	V01	-	A	7058	78	03	V01	351A-064	S
27PS49	16	67	V01	-	S						

Table 1-1. Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Code		Software Version	Adapter	Approval Status	Device Part Number	Family and Pinout Code		Software Version	Adapter	Approval Status
Fujitsu (Cont.)						Harris Semiconductor (Cont.)					
7115	68	03	V01	351A-064	S	7681RP	05	16	V01	-	A
7116	68	03	V01	351A-064	S	7684	05	06	V01	351A-064	A
7123	68	09	V01	351A-064	S	7684P	05	06	V01	351A-064	A
7124	68	09	V01	351A-064	S	7685	05	06	V01	351A-064	A
7125	68	15	V01	-	S	7685P	05	06	V01	351A-064	A
7126	68	15	V01	-	S	7616	05	42	V01	-	A
7054	78	05	V01	351A-064	S	76160	05	21	V01	-	A
7059	78	05	V01	351A-064	S	76161	05	21	V01	-	A
7121	68	05	V01	351A-064	S	76165	05	53	V01	351A-064	A
7122	68	05	V01	351A-064	S	76320	05	63	V01	-	A
7055	78	69	V01	-	S	76321	05	63	V01	-	A
7060	78	69	V01	-	S	76641	05	67	V01	-	A
7131	68	16	V01	-	S	Hitachi					
7132	68	16	V01	-	S	25044	74	05	V01	351A-064	S
7127	68	06	V01	351A-064	S	25045	74	05	V01	351A-064	S
7128	68	06	V01	351A-064	S	25088	74	16	V01	-	S
7137	68	21	V01	-	S	25088S	66	16	V01	-	S
7138	68	21	V01	-	S	25089	74	16	V01	-	S
7151	68	53	V01	351A-064	S	25089S	66	16	V01	-	S
7152	68	53	V01	351A-064	S	25084	74	06	V01	351A-064	S
7141	68	63	V01	-	S	25084S	66	06	V01	351A-064	S
7142	68	63	V01	-	S	25085	74	06	V01	351A-064	S
7143	68	67	V01	-	S	25085S	66	06	V01	351A-064	S
7144	68	67	V01	-	S	25168	74	21	V01	-	S
8518	21	27	V01	-	S	25168S	66	21	V01	-	S
8516	19	23	V01	-	S	25169	74	21	V01	-	S
8742	50	57	V01	351A-075	S	25169S	66	21	V01	-	S
8749H	50	57	V01	351A-075	S	27C32	19	24	V01	-	S
2732A	27	24	V01	-	S	27C32A	27	24	V01	-	S
2732A-35	27	24	V01	-	S	462716	19	23	V01	-	S
8532	19	24	V01	-	S	48016	33	23	V01	-	S
2764	45	33	V01	-	S	462532	19	25	V01	-	S
27128	45	51	V01	-	S	462732	19	24	V01	-	S
General Instruments						462732P	19	24	V01	-	S
5716	83	23	V01	-	S	482732A	27	24	V01	-	S
5816	37	23	V01	-	S	482764	79	33	V01	-	S
Harris Semiconductor						4827128	79	51	V01	-	S
6641	40	47	V01	-	S	Hughes					
7602	05	02	V01	351A-064	A	3004-1	58	62	V01	-	S
7603	05	02	V01	351A-064	A	3004-2	58	61	V01	-	S
7610	05	01	V01	351A-064	A	3704-1	58	62	V01	-	S
7611	05	01	V01	351A-064	A	3704-2	58	61	V01	-	S
7629	05	43	V01	-	A	3008	58	60	V01	-	S
7620	05	03	V01	351A-064	A	3708	58	60	V01	-	S
7621	05	03	V01	351A-064	A	Intel					
7640	05	15	V01	-	A	2704	21	26	V01	-	O
7641	05	15	V01	-	A	8704	21	26	V01	-	O
7648	05	09	V01	351A-064	A	2708	21	27	V01	-	O
7649	05	09	V01	351A-064	A	2758	19	22	V01	-	O
7642	05	05	V01	351A-064	A	8708	21	27	V01	-	O
7642P	05	38	V01	351A-064	A	8741	56	59	V01	351A-075	S
7643	05	05	V01	351A-064	A	8741A	56	59	V01	351A-075	S
7643P	05	38	V01	351A-064	A	8748	52	56	V01	351A-075	A
7608	05	16	V01	-	A	8748H	50	56	V01	351A-075	A
7680	05	16	V01	-	A	2716	19	23	V01	-	A
7680RP	05	16	V01	-	A	2815	85	23	V01	-	A
7681	05	16	V01	-	A						

Table 1-1. Family and Pinout Codes (Continued)

Device Part Number	Family end Pinout Code	Software Version	Adepter	Approval Status	Device Part Number	Family end Pinout Code	Software Version	Adepter	Approval Status
<b>Intel (Cont.)</b>					<b>Monolithic Memories, Inc. (Cont.)</b>				
2816	37 23	V01	-	A	6306	11 03	V01	351A-064	S
8742	50 57	V01	351A-075	S	63LS240	18 03	V01	351A-064	S
8749H	50 57	V01	351A-075	A	63LS241	18 03	V01	351A-064	S
8755A	47 55	V01	351A-075	S	63S240	18 03	V01	351A-064	S
2732	19 24	V01	-	A	63S241	18 03	V01	351A-064	S
2732A	27 24	V01	-	A	5340	11 15	V01	-	S
8751	53 58	V01	351A-076	A	5340JS	11 15	V01	351A-074	S
2764	79 33	V01	-	A	5341	11 15	V01	-	S
27128	79 51	V01	-	A	5341JS	11 15	V01	351A-074	S
27256	93 32	V01	-	A	5348	11 09	V01	351A-056	S
<b>Intersil</b>					5349	11 09	V01	351A-064	S
5600	70 02	V01	351A-064	O	6340	11 15	V01	-	S
5610	70 02	V01	351A-064	O	6340JS	11 15	V01	351A-074	S
5603A	70 01	V01	351A-064	O	6341	11 15	V01	-	S
5623	70 01	V01	351A-064	O	6341JS	11 15	V01	351A-074	S
5604	70 03	V01	351A-064	O	6348	11 09	V01	351A-064	S
5624	70 03	V01	351A-064	O	6349	11 09	V01	351A-064	S
6716	59 64	V01	-	A	63S480	18 09	V01	351A-064	O
<b>Mitsubishi</b>					63S481	18 09	V01	351A-064	O
2708	21 27	V01	-	S	5352	11 05	V01	351A-064	S
8748	52 56	V01	351A-075	S	5353	11 05	V01	351A-064	S
2716	19 23	V01	-	S	6352	11 05	V01	351A-064	S
2732	19 24	V01	-	S	6353	11 05	V01	351A-064	S
2732A	27 24	V01	-	S	63LS441	18 05	V01	351A-064	O
2764	79 33	V01	-	S	63RA441	18 07	V01	351A-064	S
27128	79 51	V01	-	S	63RD441	18 07	V01	351A-064	S
<b>Monolithic Memories, Inc.</b>					63RS441	18 07	V01	351A-064	O
5330	29 02	V01	351A-064	A	63S440	18 05	V01	351A-064	S
5331	29 02	V01	351A-064	A	63S441	18 05	V01	351A-064	S
53LS080	18 02	V01	351A-064	O	5380	11 16	V01	-	S
53LS081	18 02	V01	351A-064	O	5380JS	11 16	V01	351A-074	S
53S080	18 02	V01	351A-064	A	5381	11 16	V01	-	S
53S081	18 02	V01	351A-064	A	5381JS	11 16	V01	351A-074	S
6330	29 02	V01	351A-064	A	6380	11 16	V01	-	S
6331	29 02	V01	351A-064	A	6380JS	11 16	V01	351A-074	S
63LS080	18 02	V01	351A-064	O	6381	11 16	V01	-	S
63LS081	18 02	V01	351A-064	O	6381JS	11 16	V01	351A-074	S
63S080	18 02	V01	351A-064	A	5388	11 06	V01	351A-064	S
63S081	18 02	V01	351A-064	A	5389	11 06	V01	351A-064	S
63S081	18 02	V01	351A-064	A	6388	11 06	V01	351A-064	S
5300	11 01	V01	351A-064	A	6389	11 06	V01	351A-064	S
5301	11 01	V01	351A-064	A	63RA841	18 11	V01	351A-064	O
6300	11 01	V01	351A-064	A	63S840	18 06	V01	351A-064	O
6301	11 01	V01	351A-064	A	63S841	18 06	V01	351A-064	S
63LS140	18 01	V01	351A-064	A	63S1681JS	18 21	V01	351A-074	S
63LS141	18 01	V01	351A-064	A	63PL1681	18 21	V01	-	S
63S140	18 01	V01	351A-064	A	63PS1681	18 21	V01	-	S
63S141	18 01	V01	351A-064	A	63S1680	18 21	V01	-	O
5308	11 08	V01	351A-064	S	63S1681	18 21	V01	-	S
5309	11 08	V01	351A-064	S	63S1640	18 53	V01	351A-064	O
5335	11 14	V01	-	O	63S1641	18 53	V01	351A-064	S
5336	11 14	V01	-	S	63S3281	18 63	V01	-	S
6308	11 08	V01	351A-064	S	<b>Mostek</b>				
6309	11 08	V01	351A-064	S	2716	19 23	V01	-	O
6335	11 14	V01	-	S					
6336	11 14	V01	-	S					
5305	11 03	V01	351A-064	S					
5306	11 03	V01	351A-064	S					
6305	11 03	V01	351A-064	S					

Table 1-1. Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Code		Software Version	Adepter	Approval Status	Davica Part Number	Family end Pinout Code		Software Version	Adeptar	Approval Status
Motorola						National Semiconductor (Cont.)					
7620	05	03	V01	351A-064	O	74S573	08	05	V01	351A-064	A
7621	05	03	V01	351A-064	A	77LS181	08	16	V01	-	A
7640	05	15	V01	-	O	77S180	08	16	V01	-	A
7641	05	15	V01	-	A	87LS181	08	16	V01	-	A
7649	05	09	V01	351A-064	A	87S180	08	16	V01	-	A
7642	05	05	V01	351A-064	O	87S181	08	16	V01	-	A
7643	05	05	V01	351A-064	A	87S280	08	16	V01	351A-074	S
7680	05	16	V01	-	O	87S281	08	16	V01	351A-074	S
7681	05	16	V01	-	A	77S184	08	06	V01	-	A
7684	05	06	V01	351A-064	O	77S185	08	06	V01	-	A
7685	05	06	V01	351A-064	A	87S184	08	06	V01	351A-064	A
76161	05	21	V01	-	A	87S185	08	06	V01	351A-064	A
76165	05	53	V01	351A-064	A	87S190	08	21	V01	-	A
MCM2708P	21	27	V01	-	A	87S191	08	21	V01	-	A
MCM2808	81	72	V01	-	A	87S290	08	21	V01	351A-074	S
MCM68708	21	27	V01	-	A	87S291	08	21	V01	351A-074	S
MCM2716	19	23	V01	-	A	87S195	08	53	V01	351A-064	S
MCM2816	43	23	V01	-	A	87S321	08	63	V01	-	S
MCM2817	81	71	V01	-	A	2708	21	27	V01	-	S
TMS2716	23	28	V01	-	A	2758A	19	22	V01	-	S
68732-0	25	44	V01	-	O	2758B	19	35	V01	-	S
68732-1	25	45	V01	-	O	2716	19	23	V01	-	S
MCM2532	19	25	V01	-	A	2816	37	23	V01	-	A
MCM2832	81	70	V01	-	A	9716	33	23	V01	-	A
MCM68764	25	29	V01	-	A	2532	19	25	V01	-	S
MCM68766	25	29	V01	-	A	2732	19	24	V01	-	S
Natonel Semiconductor						2764	35	33	V01	-	S
27C16	19	23	V01	-	S	Nippon Electric Company, Ltd.					
25C32	19	25	V01	-	S	B403	72	01	V01	351A-064	S
27C32	19	24	V01	-	S	B423	72	01	V01	351A-064	S
54S188	08	02	V01	351A-064	A	B405	72	15	V01	-	S
54S288	08	02	V01	351A-064	A	B425	72	15	V01	-	S
74S188	08	02	V01	351A-064	A	B406	72	05	V01	351A-064	S
74S288	08	02	V01	351A-064	A	B426	72	05	V01	351A-064	S
54S287	08	01	V01	351A-064	A	B408	72	16	V01	-	S
54S387	08	01	V01	351A-064	A	B417	72	16	V01	-	S
74S287	08	01	V01	351A-064	A	B428	72	16	V01	-	S
74S387	08	01	V01	351A-064	A	B409	72	21	V01	-	S
54LS471	08	08	V01	351A-064	A	B419	72	42	V01	-	S
54S471	08	08	V01	351A-064	A	B429	72	21	V01	-	S
74LS471	08	08	V01	351A-064	A	8741AD	56	59	V01	351A-075	S
74S471	08	08	V01	351A-064	A	8748AD	52	56	V01	351A-075	S
54S570	08	03	V01	351A-064	A	2716	19	23	V01	-	S
54S571	08	03	V01	351A-064	A	8755A	47	55	V01	351A-075	S
74S570	08	03	V01	351A-064	A	2732	19	24	V01	-	S
74S571	08	03	V01	351A-064	A	2732A	27	24	V01	-	S
54S472	08	09	V01	351A-064	A	2764	79	33	V01	-	S
54S473	08	09	V01	351A-064	A	27128	79	51	V01	-	S
54S474	08	15	V01	-	A	Oki					
54S475	08	15	V01	-	A	2708	21	27	V01	-	S
74S472	08	09	V01	351A-064	A	2758	19	22	V01	-	S
74S473	08	09	V01	351A-064	A	2716	19	23	V01	-	S
74S474	08	15	V01	-	A	8755A	47	55	V01	351A-075	S
74S475	08	15	V01	-	A	2532	19	25	V01	-	S
87S295	08	15	V01	-	A	2732	19	24	V01	-	S
87S296	08	15	V01	-	A	2732A	27	24	V01	-	S
54S572	08	05	V01	351A-064	A	2764	79	33	V01	-	S
54S573	08	05	V01	351A-064	A	27128	79	51	V01	-	S
74S572	08	05	V01	351A-064	A						

Table 1-1. Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Code		Software Version	Adapter	Approval Status	Device Part Number	Family and Pinout Code		Software Version	Adapter	Approval Status
Reytheon						SGS					
29660	11	01	V01	351A-064	A	2716	19	23	V01	-	S
29661	11	01	V01	351A-064	A	2732	19	24	V01	-	S
29662	11	01	V01	351A-064	A	Signetics					
29663	11	01	V01	351A-064	A	82123	10	02	V01	351A-064	O
29600	11	08	V01	351A-064	A	82S123	10	02	V01	351A-064	A
29601	11	08	V01	351A-064	A	82S23	10	02	V01	351A-064	A
29602	11	08	V01	351A-064	A	82S126	10	01	V01	351A-064	A
29603	11	08	V01	351A-064	A	82S129	10	01	V01	351A-064	A
29610	11	03	V01	351A-064	A	82S130	10	03	V01	351A-064	A
29611	11	03	V01	351A-064	A	82S131	10	03	V01	351A-064	A
29612	11	03	V01	351A-064	A	82S140	10	15	V01	-	A
29613	11	03	V01	351A-064	A	82S141	10	15	V01	-	A
29620	11	09	V01	351A-064	A	82S146	10	09	V01	351A-064	A
29621	11	09	V01	351A-064	A	82S147	10	09	V01	351A-064	A
29622	11	09	V01	351A-064	A	82LS137	10	05	V01	351A-064	S
29623	11	09	V01	351A-064	A	82S136	10	05	V01	351A-064	A
29624	11	15	V01	-	A	82S137	10	05	V01	351A-064	A
29625	11	15	V01	-	A	82LS180	10	16	V01	-	A
29626	11	15	V01	-	A	82LS181	10	16	V01	-	A
29627	11	15	V01	-	A	82PS180	10	16	V01	-	S
29630	11	16	V01	-	A	82PS181	10	16	V01	-	S
29630SM	11	16	V01	351A-074	A	82S180	10	16	V01	-	A
29631	11	16	V01	-	A	82S181	10	16	V01	-	A
29631SM	11	16	V01	351A-074	A	82S182	10	16	V01	-	A
29632	11	16	V01	-	A	82S183	10	16	V01	-	A
29632SM	11	16	V01	351A-074	A	82S2708	10	16	V01	-	A
29633	11	16	V01	-	A	82S184	10	06	V01	351A-064	A
29633SM	11	16	V01	351A-074	A	82S185	10	06	V01	351A-064	A
29634	11	16	V01	-	A	82S190	10	21	V01	-	A
29635	11	16	V01	-	A	82S191	10	21	V01	-	A
29636	11	16	V01	-	A	82S195	10	53	V01	351A-064	A
29637	11	16	V01	-	A	82S321	10	63	V01	-	A
29660	11	06	V01	351A-064	A	2708	21	27	V01	-	S
29651	11	06	V01	351A-064	A	Synertek					
29652	11	06	V01	351A-064	A	2716	19	23	V01	-	O
29653	11	06	V01	351A-064	A	Texas Instruments					
29680	11	21	V01	-	A	24S10	13	01	V01	351A-064	A
29680SM	11	21	V01	351A-074	A	24SA10	13	01	V01	351A-064	A
29681	11	21	V01	-	A	28L22	13	46	V01	351A-064	A
29681SM	11	21	V01	351A-074	A	28LA22	13	46	V01	351A-064	A
29682	11	21	V01	-	A	28L42	13	09	V01	351A-064	A
29682SM	11	21	V01	351A-074	A	28L45	13	15	V01	351A-074	A
29683	11	21	V01	-	A	28P42	13	09	V01	351A-064	A
29683SM	11	21	V01	351A-074	A	28P45	13	15	V01	351A-074	A
29640	11	53	V01	351A-064	A	28S42	13	09	V01	351A-064	A
29641	11	53	V01	351A-064	A	28S45	13	15	V01	351A-074	S
29642	11	53	V01	351A-064	A	28S46	13	15	V01	351A-074	A
29643	11	53	V01	351A-064	A	28SA42	13	09	V01	351A-064	A
29671	11	63	V01	-	A	28SA46	13	15	V01	351A-074	A
29673	11	63	V01	-	A	24S41	13	38	V01	351A-064	A
Ricoh						24SA41	13	38	V01	351A-064	A
RD5H32	27	24	V01	-	S	54S476	13	38	V01	351A-064	O
Seeq						54S477	13	38	V01	351A-064	O
5133	35	33	V01	-	S	74S476	13	38	V01	351A-064	O
5133H	79	33	V01	-	S	74S477	13	38	V01	351A-064	O
						28L85	13	16	V01	351A-074	A

Table 1-1. Family and Pinout Codes (Continued)

Device Part Number	Family end Pinout Code	Software Version	Adepter	Approval Status	Device Part Number	Family end Pinout Code	Software Version	Adepter	Approval Status		
Texas Instruments (Cont.)					Texas Instruments (Cont.)						
28L86	13	16	V01	-	A	2708	21	27	V01	-	A
28P85	13	16	V01	351A-074	A	27L08	21	27	V01	-	A
28S2708	13	16	V01	-	A	2516	31	23	V01	-	A
28S85	13	16	V01	351A-074	A	TMS2716	23	28	V01	-	A
28S86	13	16	V01	-	A	2532	31	25	V01	-	A
28SA86	13	16	V01	-	A	25L32	19	25	V01	-	A
54LS478	13	16	V01	-	O	2732	31	24	V01	-	A
54S478	13	16	V01	-	O	2732A	27	24	V01	-	A
54S479	13	16	V01	-	O	2564	31	30	V01	-	A
74LS478	13	16	V01	-	O	2764	35	33	V01	-	A
74S2708	13	16	V01	-	O	Toshiba					
74S478	13	16	V01	-	O	321	21	26	V01	-	A
74S479	13	16	V01	-	O	322	21	27	V01	-	A
24S81	13	06	V01	351A-064	A	323	19	23	V01	-	S
24SA81	13	06	V01	351A-064	A	8755AC	47	55	V01	351A-075	S
74S454	13	06	V01	351A-064	O	2732	19	24	V01	-	A
74S455	13	06	V01	351A-064	O	2732A	27	24	V01	-	A
28L166	13	21	V01	-	A	2732D	19	24	V01	-	S
28P166	13	21	V01	-	A	2764	79	33	V01	-	S
28S166	13	21	V01	-	A	27128	79	51	V01	-	S
28SA166	13	21	V01	-	A						
24S166	13	53	V01	351A-064	A						
24SA166	13	53	V01	351A-064	A						
2508	19	22	V01	-	A						

## KEY TO HEADINGS AND FOOTNOTES

- **Device Part Number.** The number assigned by the device manufacturer.
- **Family Code.** A 2-digit number that designates the programming algorithm.
- **Pinout Code.** A 2-digit number used to differentiate device types based on pin assignment and array size.
- **Software Version.** A number in this column specifies the earliest software version of the 22A that will program the device to the manufacturer's latest specifications.
- **Adepter.** Model number of the socket adapter that programs the device. If a number does not appear in this column, use the fixed 28-pin front panel socket to program your device.
- **Approval Status.** The following is an explanation of the symbols used in this column.

A - Written approval obtained.

- O - Device is obsolete and no longer in production. No approval can be obtained. Algorithm has been used and approved in previous Data I/O equipment.
- S - This algorithm is in the process of submission for manufacturer approval. The algorithm has been tested by Data I/O or the manufacturer, but no representation as to yield level is made or implied.

## CAUTION

Entry of an invalid family/pinout code, other than those listed in this table can cause unpredictable results at the device socket, which may damage the device. A valid family code and a valid pinout code may be combined to produce an invalid (illegal) combination. The correct combination for your device is published in this table. All family/pinout combinations not contained in this table are considered "illegal". Data I/O assumes no responsibility or liability for results produced by entry of "illegal" family/pinout combinations.

## SECTION 2

# INSTALLATION

### 2.1 INTRODUCTION

The following sections present information on how to set up your programmer for operation. Included are the following topics:

- Dust Cover Removal...section 2.2
- Inspection...section 2.3
- Power connection...section 2.4
- Power and fuse requirements...sections 2.4.1 and 2.4.2
- Installation of a socket adapter...section 2.5
- Serial I/O connection...section 2.6

### 2.2 DUST COVER REMOVAL

To gain access to your 22A, and its component pieces, you must first remove the unit's protective dust cover. To do this, refer to figure 2-1 and follow these instructions:

1. Orient the case so that the handle is facing you.
2. With your thumbs, push in on the cover release tabs.
3. Lift up the dust cover lid about two inches pulling it towards you and remove it from the programmer.

4. Lay the dust cover upside down on a flat surface. As shown in figure 2-1, the dust cover should contain an Operator Guide (12-990-0003), Power Cord (416-0010 or 416-1577) and socket adapter (optional).

#### 2.2.1 DUST COVER INSTALLATION

When you are finished using your 22A, reinstall your dust cover. Refer to figure 2-2 and follow these instructions:

1. Orient the programmer so that the handle is facing you.
2. Pick up the dust cover and insert its grab hooks into each inside vent slot in the programmer's front panel.
3. Push the dust cover in and then down so that it snaps in place.

### 2.3 INSPECTION

Your programmer was thoroughly calibrated, tested and inspected before shipment. The unit was carefully packaged to prevent damage and should arrive free of any defects and in perfect operating condition. Carefully inspect it for any damage that may have occurred during transit. If you note any damage, file a claim with the carrier and notify Data I/O. Check the operation of the unit after you have completed the installation instructions in this section.

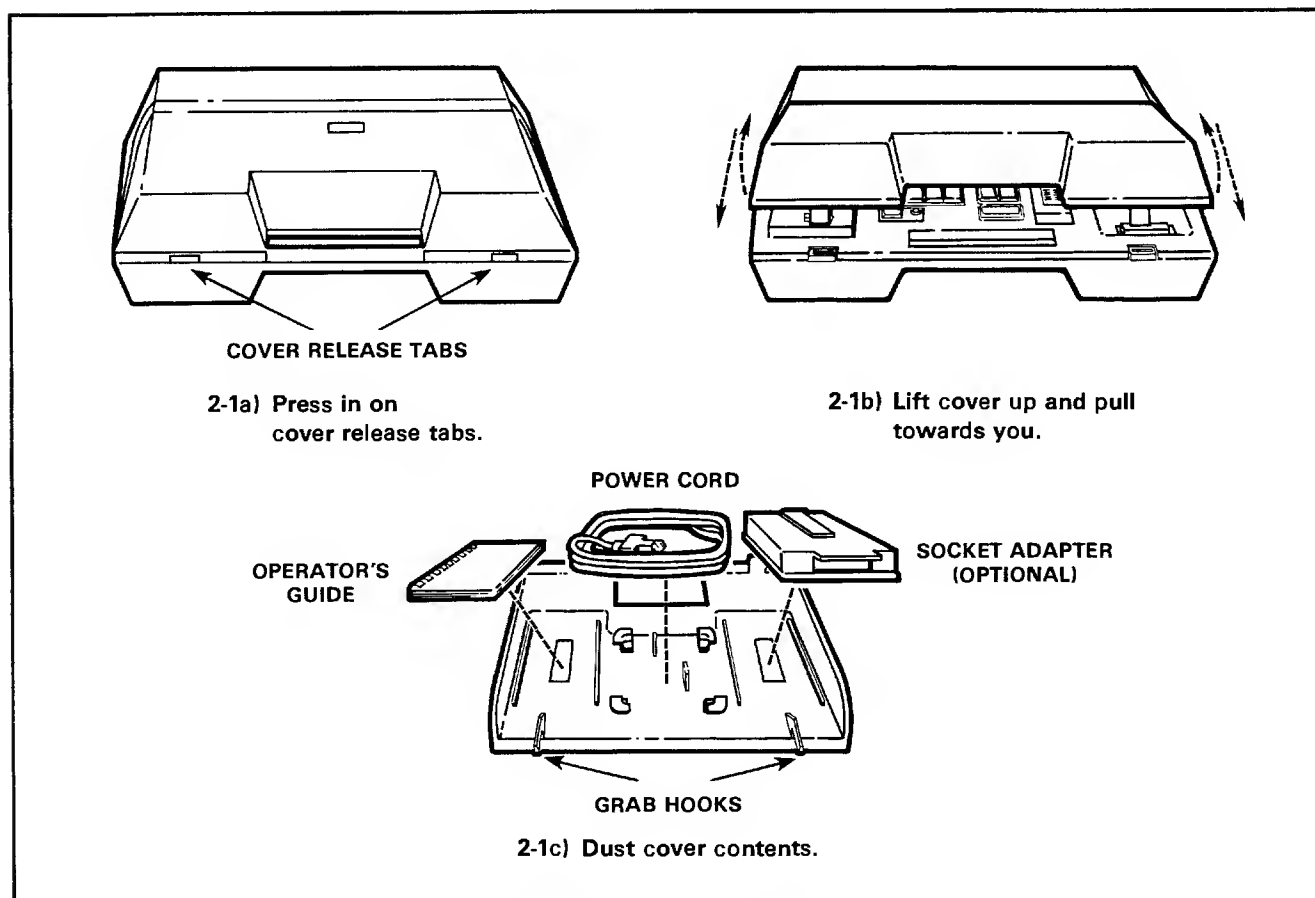


Figure 2-1. Dust Cover Removal

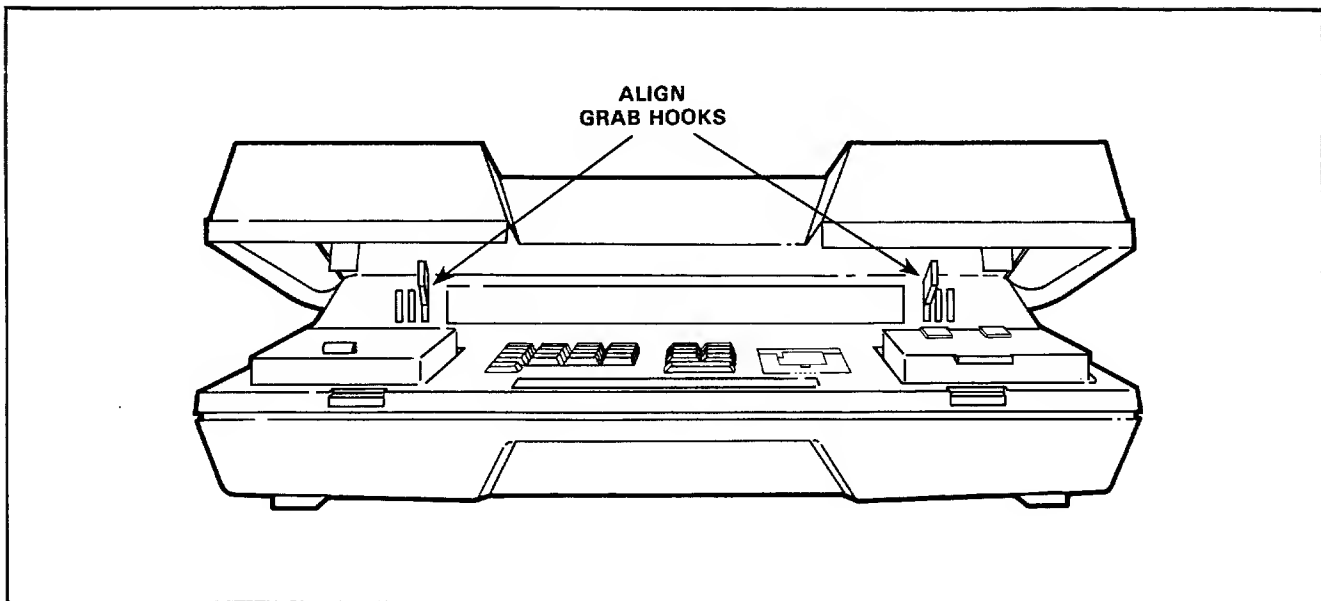


Figure 2-2. Installing the Dust Cover

Check to make sure that you have received the following required equipment:

	Data I/O Part Number	Quantity
• 22A Portable Programmer	990-0003	1
• 351A-064 Socket Adapter	715-1724	1
• Power Cord	416-0010 or, 416-1577	1
• Instruction Manual	10-990-0003	1
• Operator's Guide	12-990-0003	1

## 2.4 POWER CONNECTION

Before applying power to your programmer, make sure that the operating voltage is correct (section 2.4.1), that the line fuse is intact (section 2.4.2), and that the unit is properly grounded (section 2.4.3). Finally, connect your power cord and apply power to the programmer (section 2.4.4).

### 2.4.1 CHECKING THE OPERATING VOLTAGE

The factory has selected the proper voltage according to your specification. The voltage selected is visible on the rear panel AC receptacle unit. The programmer will operate when the voltage listed is within  $\pm 10\%$  of the voltage indicated on the voltage wheel selector. Verify the correct voltage setting on the wheel. Figure 2-3 shows the location of the voltage wheel selector. If the voltage that appears in

the window is incorrect, change the voltage according to the instructions below.

#### CAUTION

Do not operate the unit at voltages outside the selected range or you will damage the unit.

#### Changing the Voltage Setting

If the voltage wheel setting is incorrect, remove the wheel and reinsert it so that the proper line voltage appears in the window. Figure 2-3 and the following steps explain how to do this.

1. With a flatblade screwdriver, gently pull back on door (figure 2-3a).
2. Pull wheel out of its slot (figure 2-3b).
3. Align the wheel so that the correct line voltage points toward you (figure 2-3c).
4. Insert wheel back into mount rack.

#### NOTE

*If, at this point, you also wish to access the line fuse, go to step 2 in section 2.4.2.*

5. Close door so that it snaps in place.
6. The correct line voltage should now appear in the window (figure 2-3d).



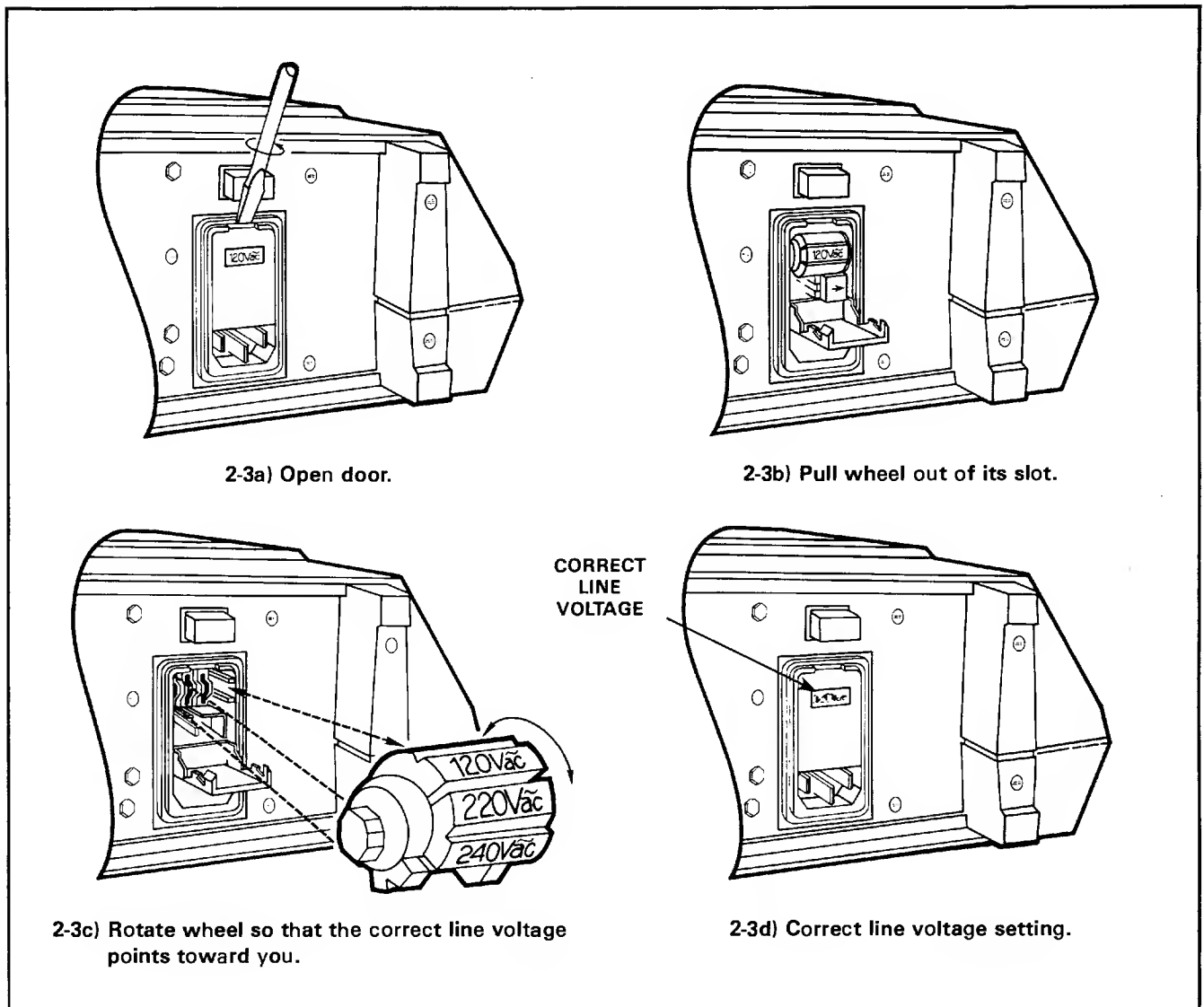


Figure 2-3. Voltage Wheel Selector

#### 2.4.2 LINE FUSE VERIFICATION

Once you have verified that your programmer is set for the correct line voltage, and is properly grounded, verify that your line fuse is intact. Check the line fuse by following these instructions and referring to the illustrations in figure 2-4:

1. With a flatblade screwdriver, gently pull open the door (figure 2-4a).
2. Pull holder tab out of slot (Figure 2-4b).
3. Check that the fuse is intact. If it needs replacing, install a new 1.5 amp fuse.
4. Insert fuse (new or existing) back into its holder.
5. Insert the fuse holder back in its slot. Once inserted, make sure that the fuse holder arrow is in the same direction as the arrows on the door (figure 2-4c).
6. Close door so that it snaps shut.

#### 2.4.3 GROUNDING THE UNIT

The power cord contains three conductors, color coded as shown in table 2-1. When the cord is connected to a three wire AC power system, the ground connector grounds the programmer's chassis, eliminating shock hazards. Do not use anything, such as a two conductor extension cord, that would break contact between the unit and an earth ground.

#### WARNING

Failure to ground the programmer may create a shock hazard. Do not defeat the three-wire power cord ground by using extension cords or adapters.

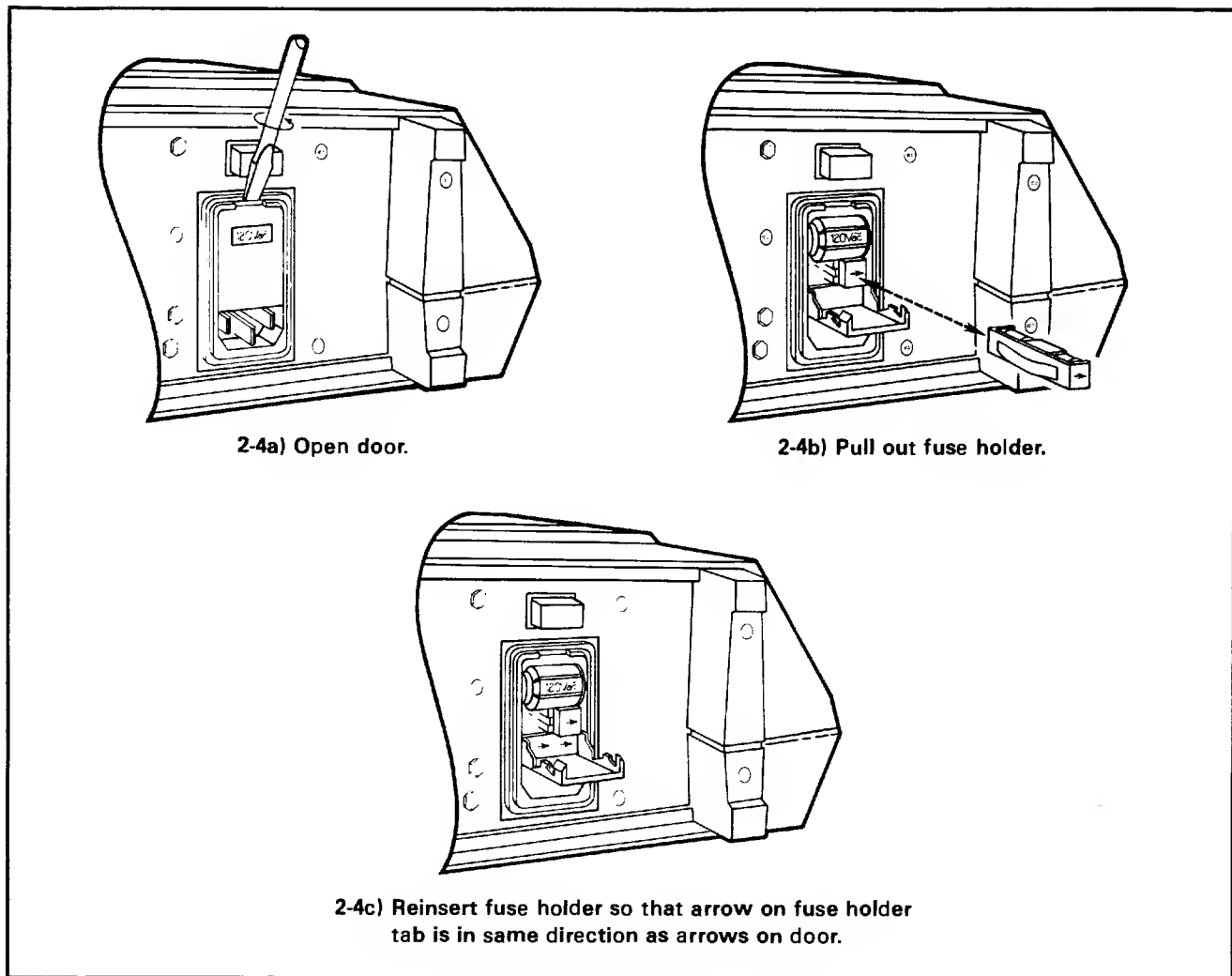


Figure 2-4. Accessing the Line Fuse

Table 2-1. Conductor Colors by Country/Continent

	U.S.A.	Europe	United Kingdom	Japan
Line	Black	Blue	Brown	Red
Neutral	White	Black	Blue	White
Ground	Green & Yellow	Green & Yellow	Green & Yellow	Black

#### 2.4.4 PLUGGING IN THE PROGRAMMER AND APPLYING POWER

Now that you have verified that the power system is in working condition, plug in your unit and apply power. The ON/OFF switch is located above the voltage selector wheel on the programmers rear panel. A step-by-step power-up procedure is located in section 3.2.

## 2.5 INSTALLING A SOCKET ADAPTER

Some devices require that you use a special socket adapter for programming related operations. The specific socket adapter to use for the operation is listed in table 1-1.

This section contains instructions on how to install that socket adapter into the front panel socket adapter receptacle. Refer to figure 2-5 for complete instructions.

1. Orient socket adapter over front panel socket receptacle.
2. Insert socket adapter flange into receptacle opening and push forward.
3. Push down socket adapter wing handle so that the socket adapter connector mates with the receptacle connector.

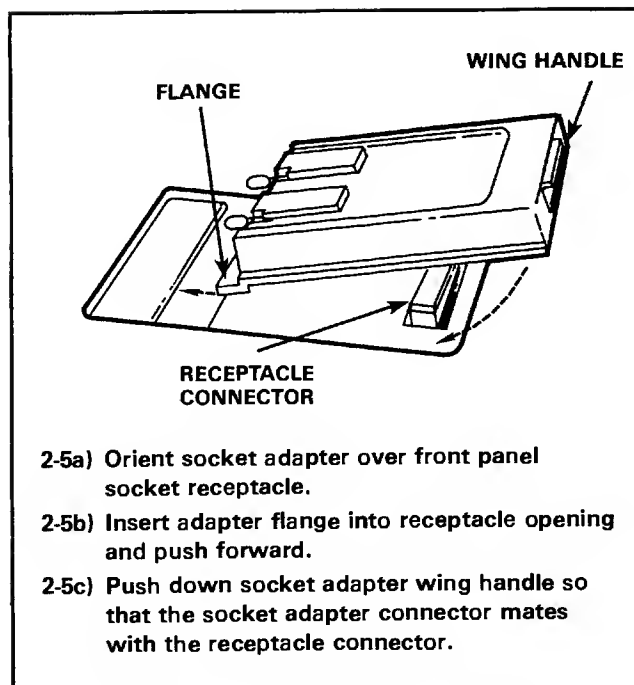


Figure 2-5. Installing a Socket Adapter

## 2.5.1 REMOVING SOCKET ADAPTER

Removing a socket adapter is a simple procedure. Follow the instructions in figure 2-6.

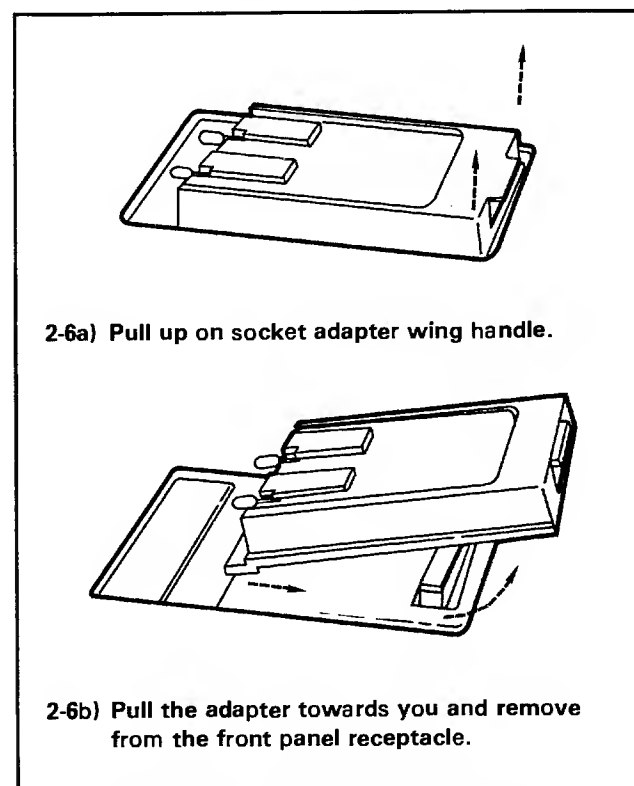


Figure 2-6. Removing a Socket Adapter

## 2.6 SERIAL I/O OPERATIONS

An RS232C serial port interface is used to connect the programmer to computer systems and other peripherals. This requires setting up the proper serial interface cabling and setting the appropriate operational parameters.

### 2.6.1 CABLING

To connect the 22A to other instruments, you must follow the RS232C specifications provided in table 2-2.

Table 2-2. Serial Interface Connector Pin Assignment

PIN NO.	SIGNAL MNEMONIC	DESCRIPTION
1.	Ground	In the RS232C environment this line is common for the $-12\text{ V}$ and provides a safety ground connection to the RS232C-compatible terminal.
2	Send Data	Transmits data within RS232C voltage levels ( $+12\text{ V}$ and $-9\text{ V}$ ).
3	Receive Data	Accepts data within RS232C voltage levels.
4	Request to Send	This line is normally held high by the programmer. It is dropped to inhibit data transmission from a remote source.
5	Clear to Send*	A high level on this line allows the programmer to transfer data. A low level inhibits data transfer.
6	Data Set Ready*	A low inhibits data transfer by programmer.
7	Signal Ground	This line provides a common signal connection to the RS232C remote source.
8	Carrier Detect*	A low inhibits data transfer by programmer.
9	+24 VDC	Available for serial paper tape reader. 600 mA maximum. This supply is automatically enabled anytime a COPY (or VERIFY) PORT to RAM operation is executed.
10-19		Not used.
20	Data Terminal Ready	Normally held high by programmer.
21		Not used.
22	+5VDC	Available for external use if required. 500 mA maximum.
23	-5VDC	Available for external use if required. 20mA maximum.
24, 25		Not used.

\*Pins 5, 6 and 8 have internal pull ups and need no connection if unused.

Figure 2-7 shows sample interconnections utilizing the RS232C interface. In general a 3-wire hook-up without handshaking is sufficient. If the peripheral's response time is slow, a 5-wire hook-up with handshaking may be used.

## 2.6.2 SETTING PARAMETERS

Before executing any I/O related operations, make sure you have set the following parameters: baud rate, stop bits and parity.

Each of these parameters is set by executing a select function. A complete list of select codes are described in table 3-2. The select function codes for setting parameters are:

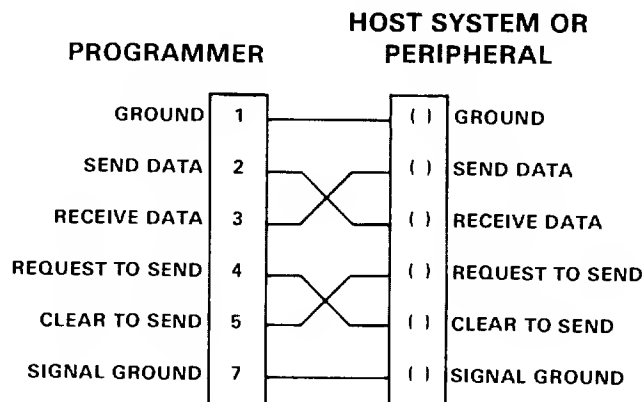
Select Code	Select Function Name
-------------	----------------------

- |      |                  |
|------|------------------|
| • DA | Set Baud Rate    |
| • DB | Select Parity    |
| • DC | Select Stop Bits |

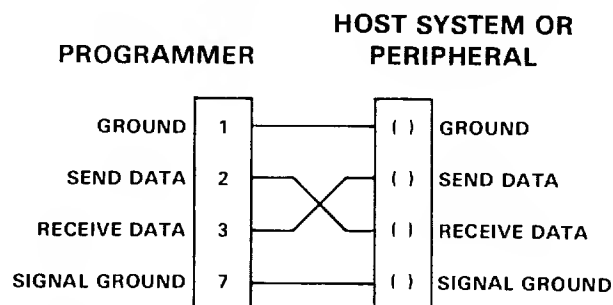
Here is how to set the desired parameter for each select function listed above.

### Key Sequence

1. Press SELECT.
2. Enter parameter's select code - see list in previous paragraph.
3. Keep pressing SELECT until you have stepped to the desired parameter value.
4. Press START.



2-7a) RS232C Connection, Half/Full Duplex, with Handshake



2-7b) RS232C Connection, Half/Full Duplex, without Handshake

### NOTES:

1. All signals are named with respect to the originating unit.
2. All undesignated pins are to be left open.
3. For applications that do not require handshaking, the programmer's clear to send line is pulled up internally.

Figure 2-7. Sample Interconnection Methods

### Power Down Save Mode

Once the parameters are set, they can be stored for future use. This is accomplished by using the power down save select function. Refer to table 3-2 for instructions on how to execute this select function.

### 2.6.3 HOOKING UP A SERIAL PAPER TAPE READER

A Data I/O Serial Paper Tape Reader (950-1950) can be hooked up to your programmer. A direct connection, to the programmer's serial port, is made using the existing serial paper tape reader cable. It will connect according to the specifications in figure 2-8. Set the baud rate at 2400. Two operations are possible using the serial paper tape reader: input from port and input verify. Refer to section 3.4.

#### NOTE

*The Paper Tape Reader cannot be operated while the UV lamp is on.*

## 2.7 REPACKAGING FOR SHIPMENT

If the instrument is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identify the owner. In correspondence, identify the unit serial number, mode number and name.

We suggest that you use the original shipping container. Place the instrument in the container with appropriate packing material and seal the container with strong tape. If you use some other container, be sure that it is a heavy and durable carton. Wrap it with sturdy paper or plastic. Use the appropriate packing material and seal the carton with strong tape. Mark the container "DELICATE" or "FRAGILE".

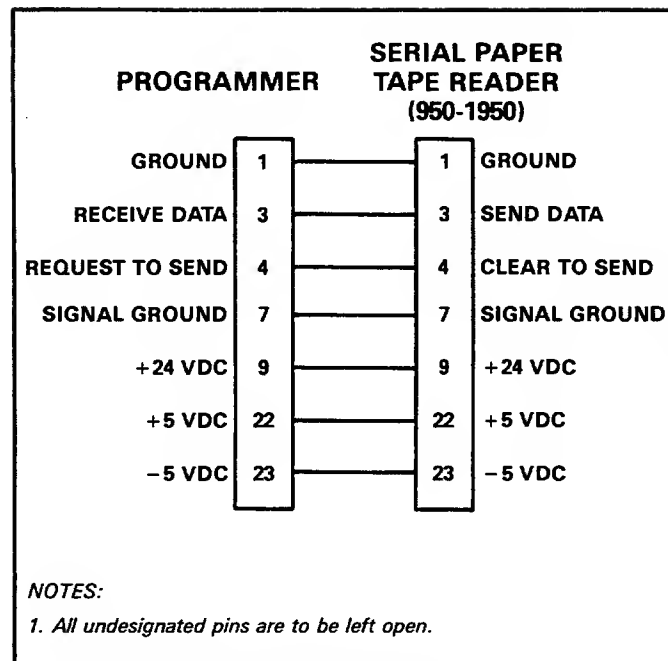


Figure 2-8. Interconnection Method for Serial Paper Tape Reader

## SECTION 3

# OPERATION

### 3.1 OVERVIEW

This section contains procedures for executing the basic operations of your 22A programmer. The 22A can obtain data to perform these operations from any of three sources: a master device, the serial port or data entered from the front panel keyboard. The basic operations of the 22A are:

1. Copy—moving data from a source (device, RAM or Port) to a destination (device, RAM or Port). The specific copy operations are:
  - Load RAM with master device data. Section 3.4.4.
  - Input from Port. Section 3.4.5.
  - Program Device. Section 3.4.6.
  - Output to Port. Section 3.4.7.
  - Block Move. Section 3.4.8.
2. Verify—comparing data between a source and destination. The verify operations include:
  - Verify Device. Section 3.4.9.
  - Input verify. Section 3.4.10.
3. Edit—changing data at selected addresses within the programmer RAM. The edit operation is documented in section 3.4.11.
4. Select Function—Allows you to either manipulate RAM data or change various operating parameters. These functions are listed and described in section 3.5.

These operations and their uses are further described in section 1.2 Theory of Operation. All copy and verify operations are presented in this section in both an operational flowchart and step-by-step key sequence format. Copy and verify operations follow the source/destination method of data transfer and verification. This concept is explained in section 3.7.

### 3.2 POWER-UP

To power-up your 22A for operation, follow these procedures:

1. Check to make sure a device is not in the front panel's fixed 28-pin socket or socket adapter. If a device is in the socket, lift up the socket locking arm (see figure 3-2) and remove the device from the socket.
2. Connect to AC power.
3. Depress the power switch to the ON position. Figure 3-1 shows the power switch location and indicates the ON position. The ON position has been achieved when a green "eye" appears inside the switch.

After you have turned on the programmer's power, the 22A executes a self-test routine that checks the internal bus structure, scratch RAM, firmware and data RAM. When the test is complete, and the programmer is ready for operation, the 22A displays "SELF TEST-OK".

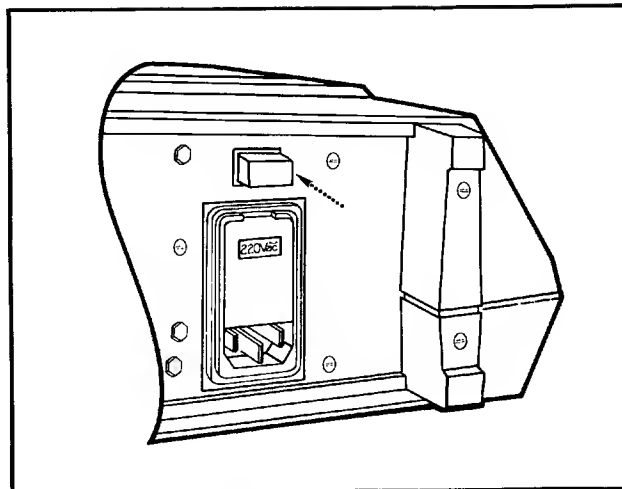


Figure 3-1. Programmer Power Switch Location


#### 3.2.1 GENERAL OPERATIONAL NOTES

Keep the following items in mind while operating the 22A:

##### Aborting an Operation

An operation can be aborted at any step in its progress by pressing one of the four mode keys (COPY, VERIFY, SELECT or EDIT). If an operation is in progress when one of these keys is pressed, the display momentarily shows the message "FUNCTION ABORT". The programmer is now in the mode selected. This abort procedure does not apply to some select functions.

##### Action Symbol

To indicate that a Copy or Verify operation is in progress, a rotating action symbol (denoted by ) appears in the display.

##### Changing a Device Related Parameter

Some operations will prompt you for information. For example, some COPY key operations will ask you for the block size or begin RAM address. Go ahead and key in this information during the operation, if necessary. Those points in an operation where you can change a value are clearly indicated on the operation's flowchart or key sequence. The following paragraph describes the programmer defaults for block size and begin RAM address. The display will prompt you with a "^" character if a value can be entered or changed.

##### Defaults

Table 3-2 identifies the default, if one exists, for select functions.

Table 3-4 identifies the default state that exists for various address parameters associated with device and port related operations.

#### **I/O Operation:**

If you are executing I/O related operations, make sure you have the correct operational parameters set. See section 2-5.

### **3.3 POWER DOWN**

#### **CAUTION**

**Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.**

To turn the programmer power off:

1. Check to make sure that the programmer is not executing an operation. If it is, wait until the operation is complete.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.4.3.
3. Depress the power switch towards the programmer (same motion you used to power-up the machine). When power has been removed from the programmer, the green "eye" no longer appears inside the power switch.

### **3.4 BASIC OPERATIONS**

The basic operations of the 22A are as follows:

- Load RAM with master device data. Section 3.4.4.
- Input from Port. Section 3.4.5.
- Program Device. Section 3.4.6.
- Output to Port. Section 3.4.7.
- Block Move. Section 3.4.8.
- Verify Device. Section 3.4.9.
- Input Verify. Section 3.4.10.
- Edit. Section 3.4.11.

Select function operations are documented in section 3.5.

#### **3.4.1 FAMILY AND PINOUT CODES**

Any device that can be programmed with the 22A is specified by a unique combination of a two digit family code and pinout code. The family and pinout codes provide the programmer with the necessary device related information such as the appropriate programming algorithm and the device's pinout architecture. Data I/O recommends that you develop the habit of entering these codes when prompted by the programmer. The codes are listed in table 1-1. Once the codes are entered for a particular device, the 22A remains set up for any operation with that device until you enter new codes.

#### **CAUTION**

**Entry of an invalid family/pinout code combination, other than those listed in table 1-1, can cause unpredictable results at the device socket which may damage the device. A valid family code and a valid pinout code may be combined to produce an invalid (illegal) combination. The correct family/pinout combination for a device can be determined by referring to table 1-1. All family/pinout combinations not contained in table 1-1 are considered illegal. Data I/O assumes no responsibility or liability for results produced by entry of illegal family/pinout code combinations.**

To select the family and pinout codes:

1. Locate the manufacturer and part number stamped on the device.
2. Go to table 1-1 and find the manufacturer's name.
3. Go to the column entitled "Device Part Number" and find the number corresponding to the number on the device.
4. Go to the columns labeled "Family Code" and "Pinout Code" to find the code numbers corresponding to the device number for the manufacturer of the device.
5. Enter the family code and pinout code you selected from this table when prompted by the programmer or terminal display. Once entered, an LED (light emitting diode) will light directly below the socket to be used in programming the device.

#### **Electronic Identifier**

The 22A can be instructed to automatically configure itself to program PROMs that have been encoded with an electronic identifier by the manufacturer.

You can do this by entering "FF" (family code) and "FF" (pinout code) at step 5 in the family and pinout code selection procedure just described. When you enter FF FF, after being prompted by the programmer for family and pinout codes, the 22A will then assemble the correct family and pinout codes for you. If you wish to check to see which family and pinout codes were selected for you by the programmer, execute select function CC DSP FAM/PIN (display family/pinout codes) in table 3-2. This select function will only work after you have initiated a device-related operation using a device which contains an electronic identifier.

#### **3.4.2 DEVICE INSERTION**

Once you have entered the appropriate family and pinout codes, the 22A is ready to accept a device in the socket which is directly above the lighted LED.

A good electrical connection between the device and the socket is essential. To ensure a good connection:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the upper-left side of the socket directly above the lighted LED; see figure 3-2. (The lever will stay in the upright position.)
3. Gently set the device in the socket directly above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket. To ensure that the device is correctly inserted, check that the bottom pins of the device mate with the bottom pins of the socket.

**NOTE**

*Make sure that 24-pin devices, which are to be inserted in the front panel's fixed 28-pin socket, are inserted into the pin 1 location shown in figure 3-2. For 16, 18 and 20 pin devices which use socket adapter 351A-064, make sure pin 1 is inserted into the correct socket pin 1 location as indicated on the top side of the socket adapter.*

4. Push the lever down to lock the device in the socket.

### 3.4.3 DEVICE REMOVAL

To remove a device:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the left side of the socket; see figure 3-2. The lever will remain in the upright position.
3. Lift the device out of the socket; the LED will remain illuminated.

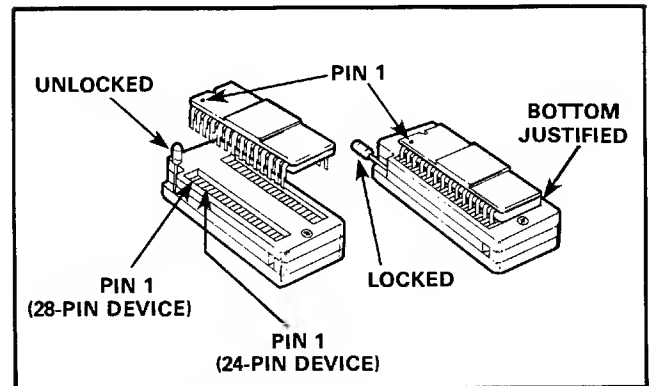
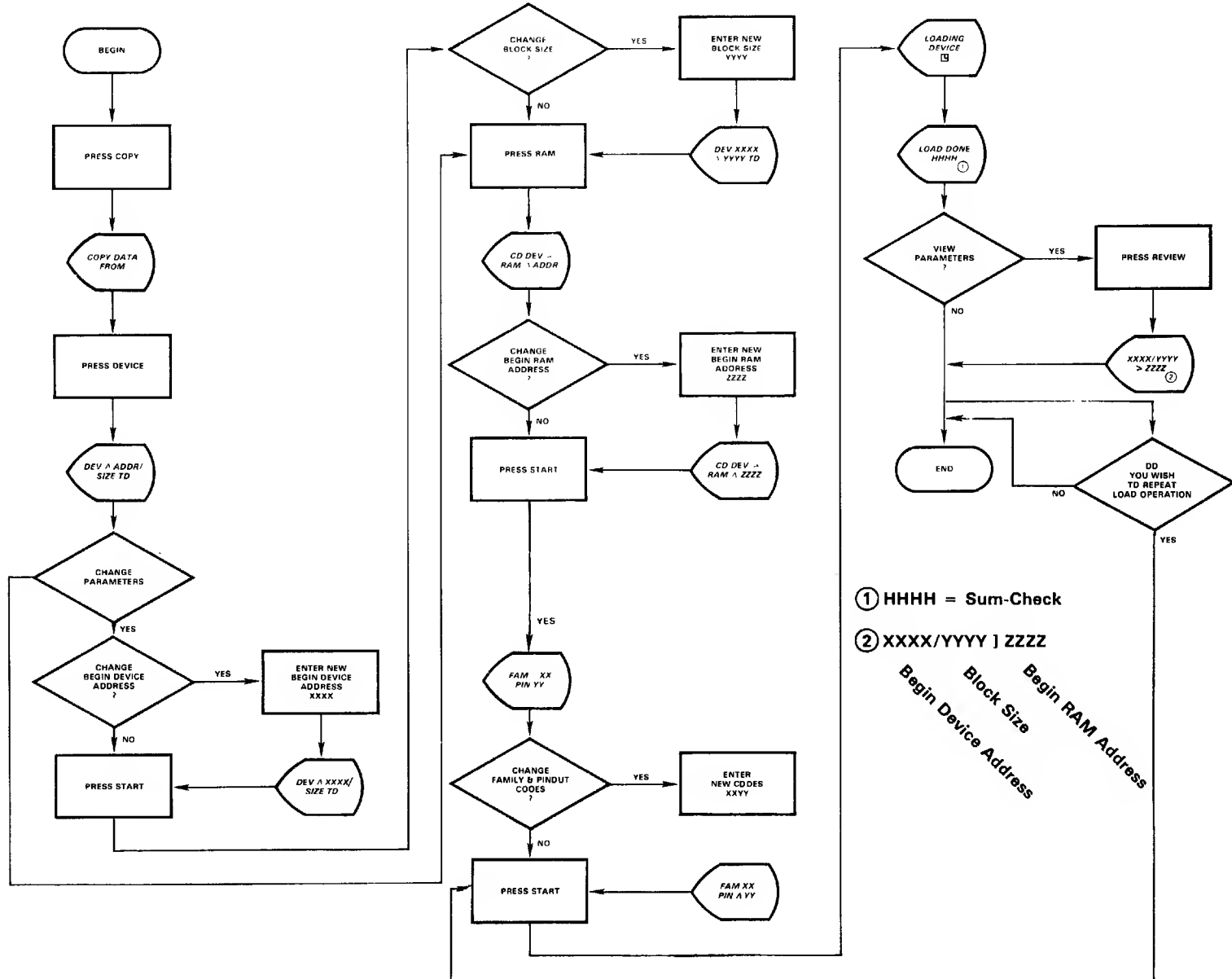


Figure 3-2. Device Installation



Figure 3-3. Load RAM with Master Device Data



### 3.4.4 LOAD RAM WITH MASTER DEVICE DATA

To load the 22A RAM with data from a master device with control from programmer front panel, follow the steps given below.

1.   to select the mode.

22A Displays

COPY DATA FROM

2.   to select the source of the data.

22A Displays

DEV^ADDR^SIZE TO



Caret in the display means that you can change the begin device address. If you do not wish to change the begin device address (or block size - step 3), go to step 4.

3.  

22A Displays

DEV^ADDR^SIZE TO

Caret next to "SIZE" means that you can change the block size.

4.   to select the destination for the data.

22A Displays

CO DEV^RAM ADDR

Enter new begin RAM address, if desired.

5.  

22A Displays

FAM^00 PIN 00

If not already displayed, enter the family code and pinout codes for the device. These codes are listed in table 1-1.

#### NOTE

The appropriate socket LED will light.

6. Insert the master device into the appropriate socket. (See section 3.4.2.)

7.  

22A Displays

LOADING DEVICE 0

LOAD DONE XXXX

#### NOTE

XXXX is the sum-check of the device.

8. Remove the master device from the socket.

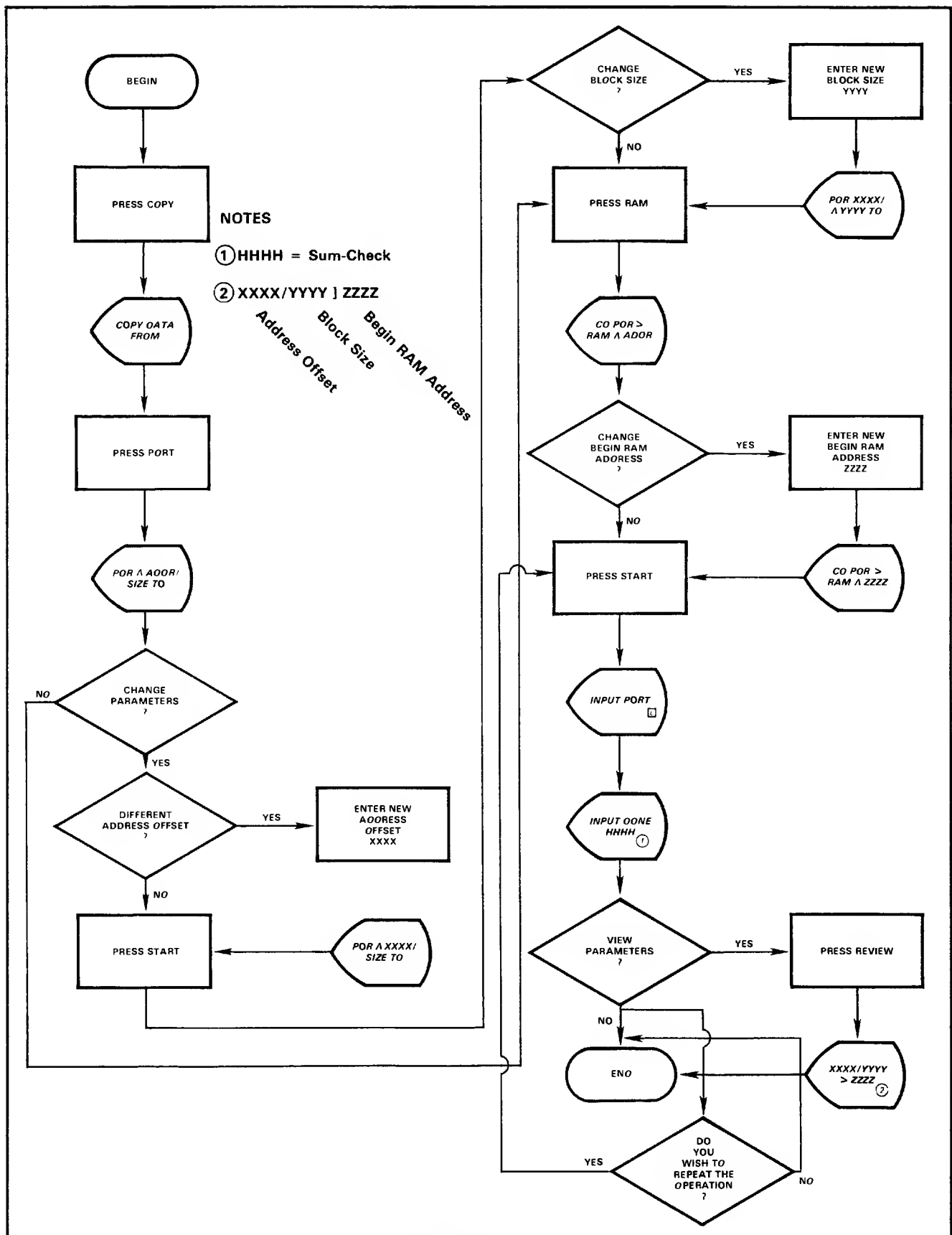


Figure 3-4. Input from Port

### 3.4.5 INPUT FROM PORT

To load the 22A RAM from front panel control, with incoming serial port data, follow the steps given below.

1. Set-up serial port. Refer to Section 2.6
2. Select the appropriate data translation format from appendix A and execute select function B3 (format number) in table 3-2.

3.   to select the mode.

22A Displays

COPY DATA FROM

4.   to select the source of data.

22A Displays

POR ^ ADDR / SIZE TO



Caret in the display means that you can change the address offset. If you do not wish to change the address offset (or block size - step 3), go to step 4.

5.  

22A Displays

POR ADDR ^ SIZE TO

Caret next to "SIZE" means that you can change the block size.

6.   to select the destination for the data.

22A Displays

CO POR ^ RAM ^ ADDR

Enter new begin RAM address, if desired.

7.  

22A Displays

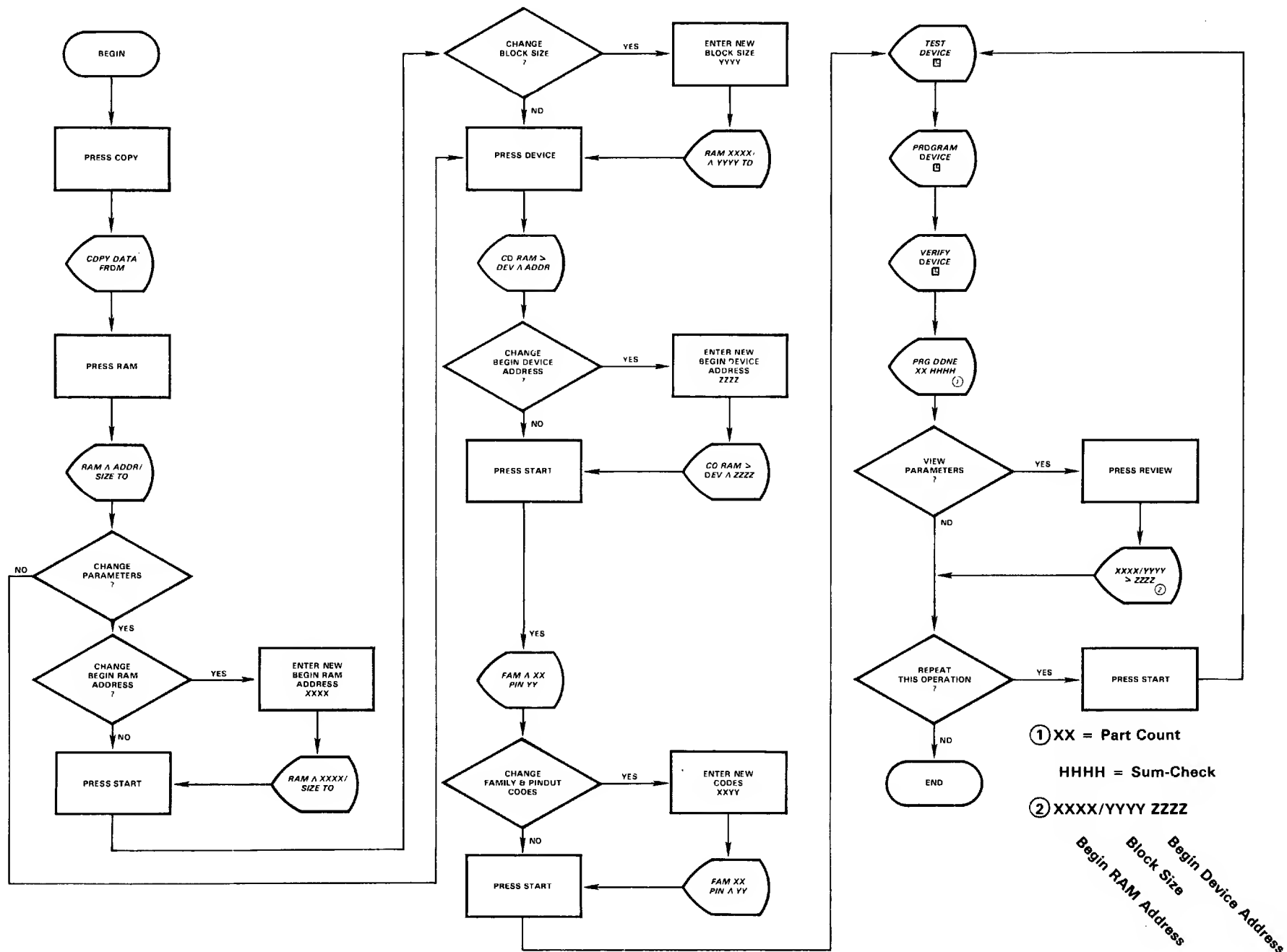
INPUT PORT 0

INPUT DONE XXXX

#### NOTE

XXXX is the sum-check of the data input from port.

Figure 3-5. Program Device



### 3.4.6 PROGRAM DEVICE WITH RAM DATA

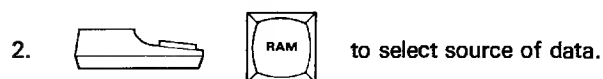
When programming a device, the system performs illegal bit tests and blank checks at nominal VCC.

To program a blank device with the data in the 22A RAM with control from the programmer front panel, follow the steps given below.



22A Displays

COPY DATA FROM



22A Displays

RAM ADDR SIZE TO

Caret in the display means that you can change the begin RAM address. If you do not wish to change the begin RAM address (or block size - step 3), go to Step 4.



22A Displays

RAM ADDR SIZE TO

Caret next to "SIZE" means that you can change the block size.



22A Displays

CO RAM DEV ADDR

Enter new begin device address, if desired.



22A Displays

FAM PIN 00

If not already displayed, enter the family and pinout codes for the device. This information is listed in table 1-1.

#### NOTE

The appropriate socket LED will light.

6. Insert the blank device into the socket.



22A Displays

TEST DEVICE 0

PROGRAM DEVICE 0

VERIFY DEVICE 0

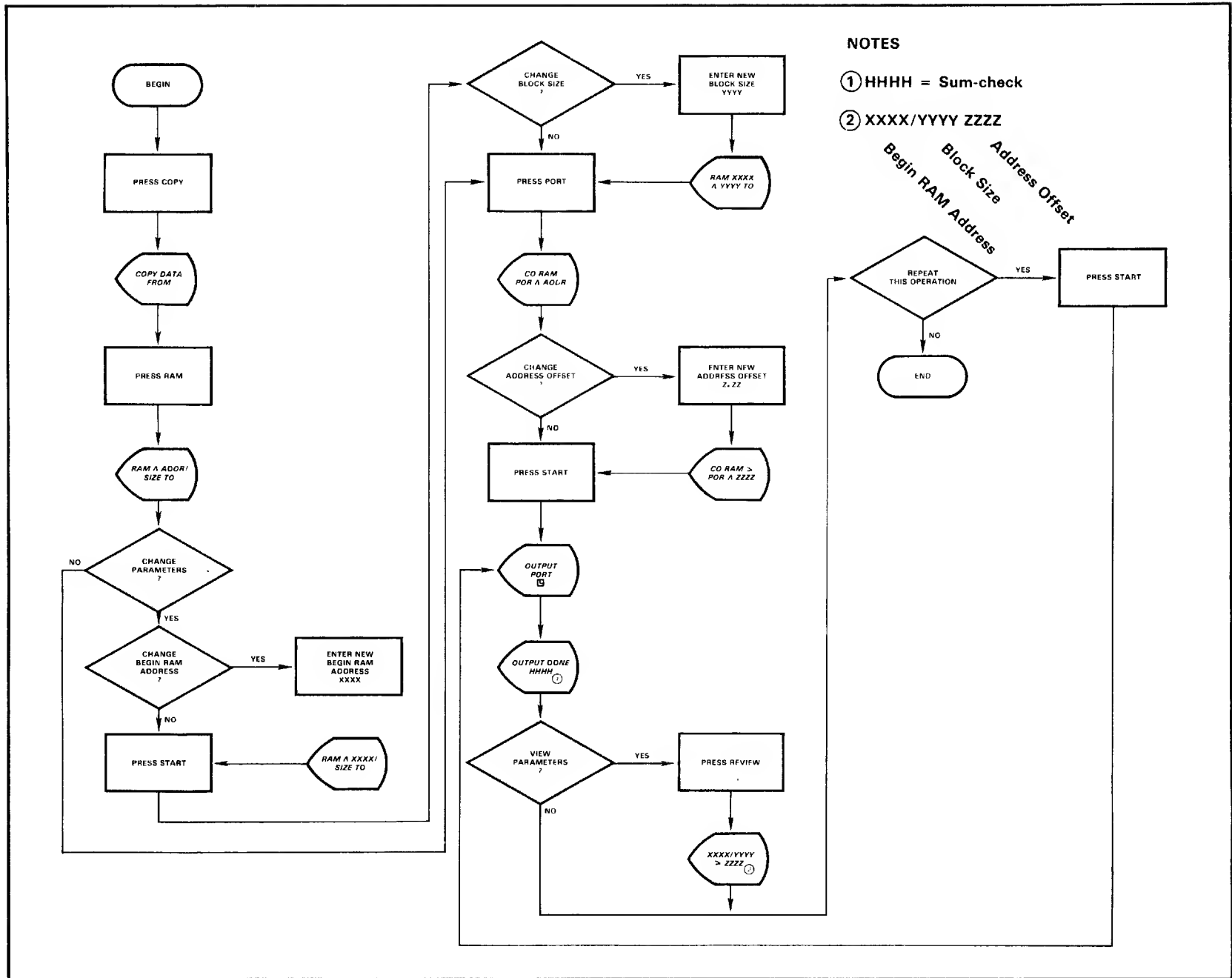
PRG DONE 01 XXXX

sequence number

sum-check

(increments by 1 for each device programmed)

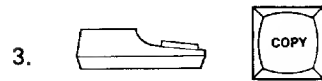
8. Remove the device from the socket.



### 3.4.7 OUTPUT TO PORT

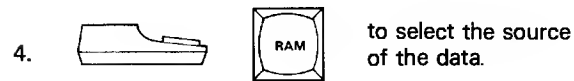
To output data to the serial port, from front panel control, follow the steps given below.

1. Set-up serial port. Refer to Section 2.6
2. Select the appropriate data translation format from Appendix A and execute select function B3 (Format Number) in table 3-2.



22A Displays

COPY DATA FROM



22A Displays

RAM ADDRESS SIZE TO

Caret in the display means that you can change the begin RAM address. If you do not wish to change the begin RAM address (or block size - step 3), go to step 4.



22A Displays

RAM ADDRESS SIZE TO

Caret next to "SIZE" means that you can change the block size.



22A Displays

CO RAM:POR ADDRESS

Enter new address offset, if desired.



22A Displays

OUTPUT TO PORT 0

OUTPUT DONE XXXX

#### NOTE

XXXX is the sum-check of data that was output to port.



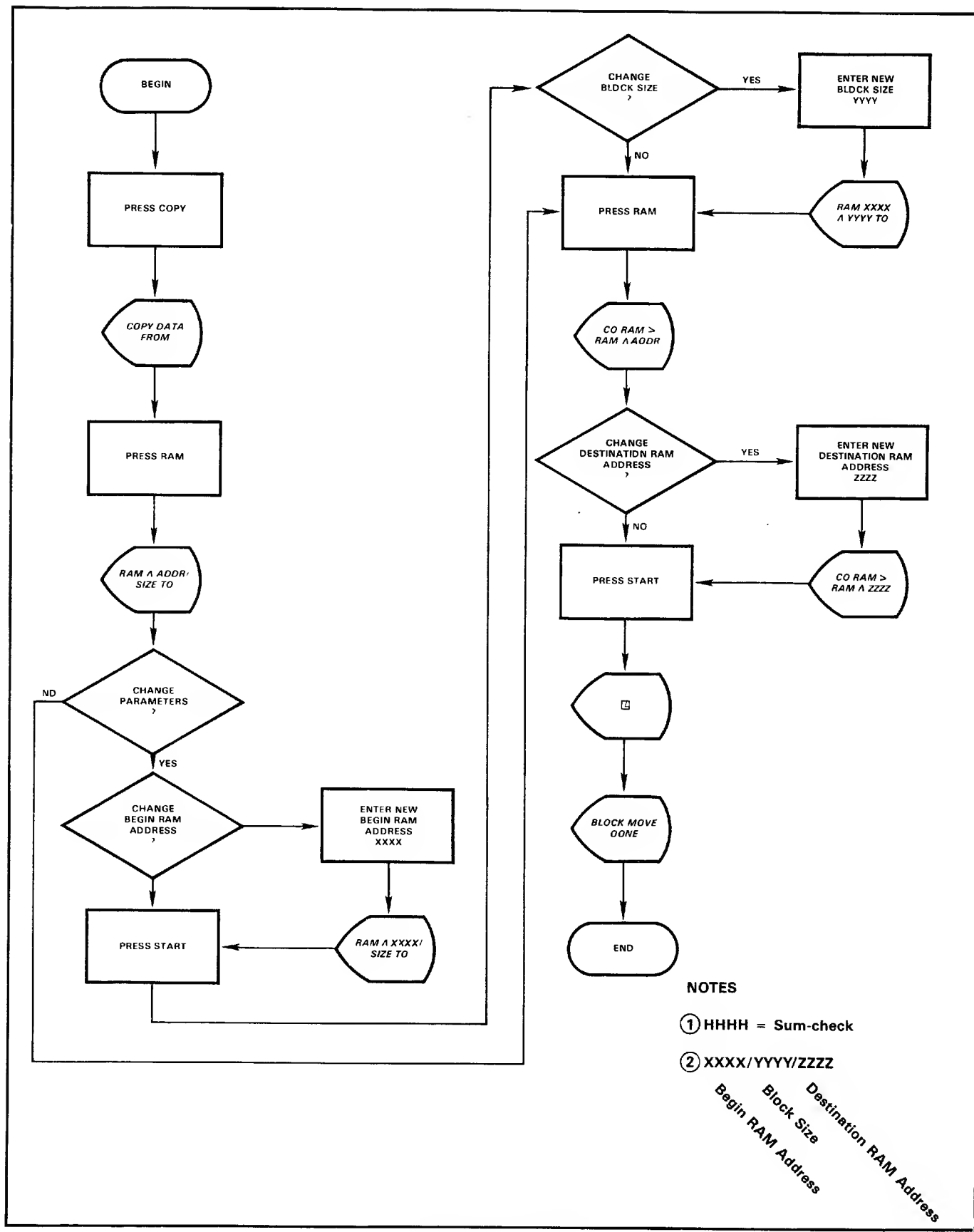


Figure 3-7. Block Move

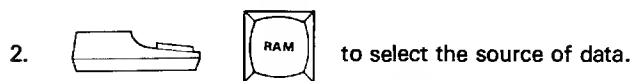
### 3.4.8 BLOCK MOVE

To move a block of data from one location in RAM to another, through front panel control, follow the steps given below.



22A Displays

COPY DATA FROM



22A Displays

RAM ADDR SIZE TO

Caret in the display means that you can change the begin RAM address. If you do not wish to change the begin RAM address (or block size - step 3), go to step 4.



22A Displays

RAM ADDR SIZE TO

Caret next to "SIZE" means that you can change the block size.



22A Displays

CO RAM RAM XXXX

Enter new destination RAM address.



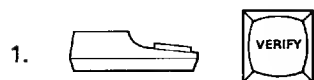
22A Displays

BLOCK MOVE 0

BLOCK MOVE DONE

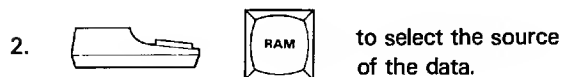
### 3.4.9 VERIFY DEVICE

To verify a device from 22A front panel control, follow the steps given below:



22A Displays

VERIFY DATA FROM



22A Displays

RAM ADDR SIZE TO

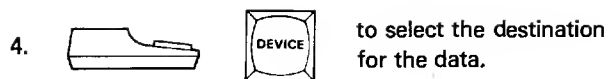
Caret in the display means that you can change the begin RAM address. If you do not wish to change the begin RAM address (or block size - step 3), go to step 4.



22A Displays

RAM ADDR SIZE TO

Caret next to "SIZE" means that you can change the block size.



22A Displays

VE DEV RAM ADDR

Enter new begin device address, if desired.



22A Displays

FAM 00 PIN 00

If not already displayed, enter the family and pinout codes for the device. This information is listed in table 1-1.

6. Insert the device to be verified in the socket which has a lit LED next to it.



22A Displays

VERIFY DEVICE 0

VE DEV DONE XXXX

**NOTE**  
XXXX is the sum-check.

8. Remove the device from the socket.

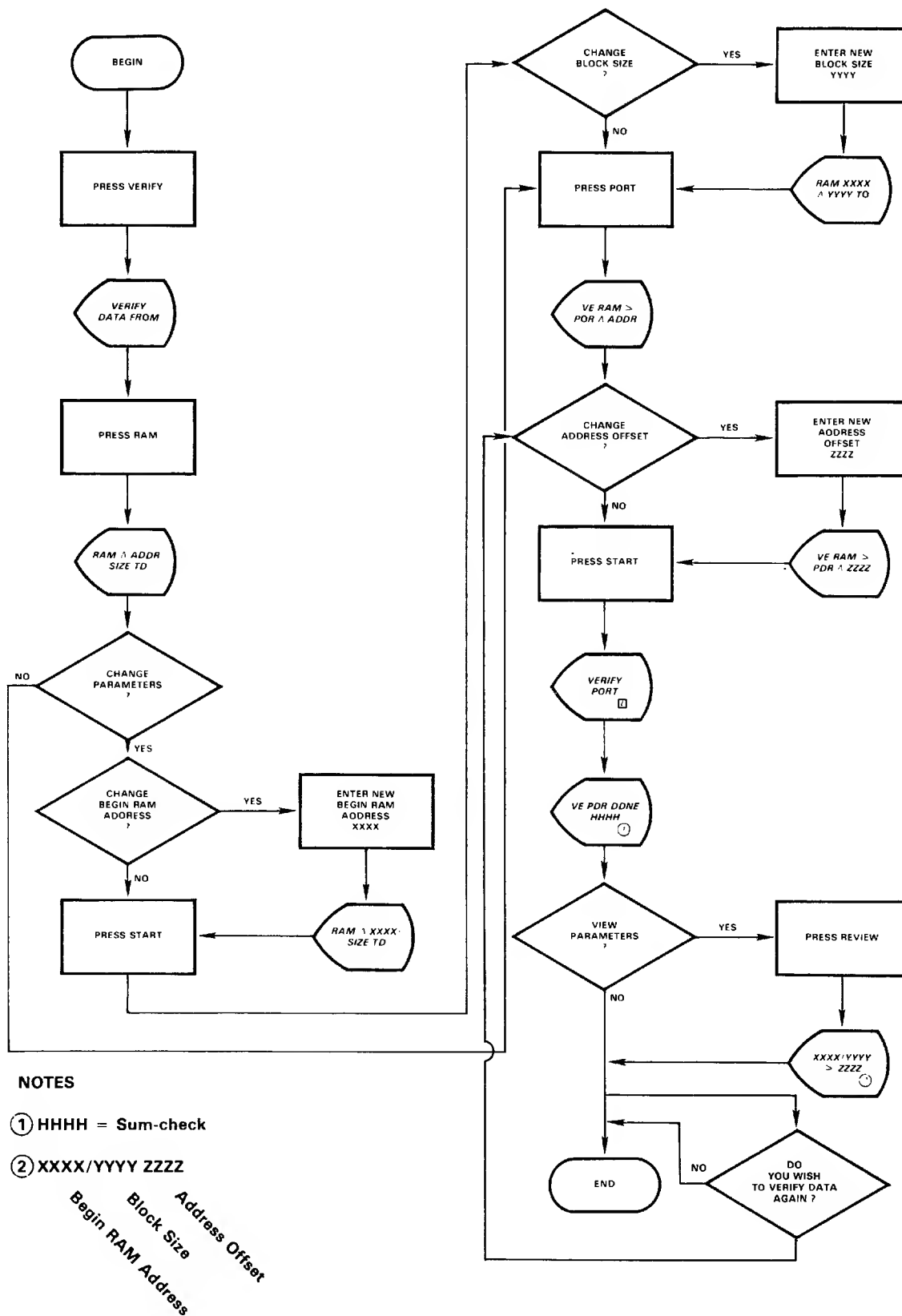


Figure 3-9. Input Verify

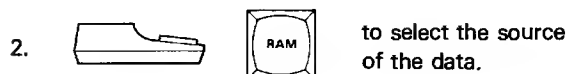
### 3.4.10 INPUT VERIFY

To verify incoming serial port data, from front panel control, follow the steps given below.



22A Displays

VERIFY DATA FROM



22A Displays

RAM ^ ADDR / SIZE TO

Caret in the display means that you can change the begin RAM address. If you do not wish to change the begin RAM address (or block size - step 3), go to step 4.



22A Displays

RAM ADDR ^ SIZE TO

Caret next to "SIZE" means that you can change the block size.



22A Displays

VE RAM:POR ^ ADDR

Enter new address offset, if desired.



22A Displays

VERIFYING PORT 0

VE POR DONE XXXX

#### NOTE

XXXX is the sum-check of the data input from the serial port.

### 3.4.11 THE EDIT KEY

The EDIT key allows you to view and change data at specified RAM addresses. Select functions F5, F6, and F7 can be used to select either binary, octal or hexadecimal number base. The desired base should be selected prior to initiating the edit operation (see table 3-2). Data may be viewed or entered from the keyboard in binary, octal or hexadecimal notation. Unless otherwise specified, the

programmer defaults to a hexadecimal number base. The edit operation is documented in figure 3-10.

Addresses are incremented one by one with the START key and decremented one by one with the REVIEW key. It is also possible to jump to any selected address by pressing the EDIT key, entering the new address and pressing START.

Edit operations take into account the previously entered device parameter for the begin device address.

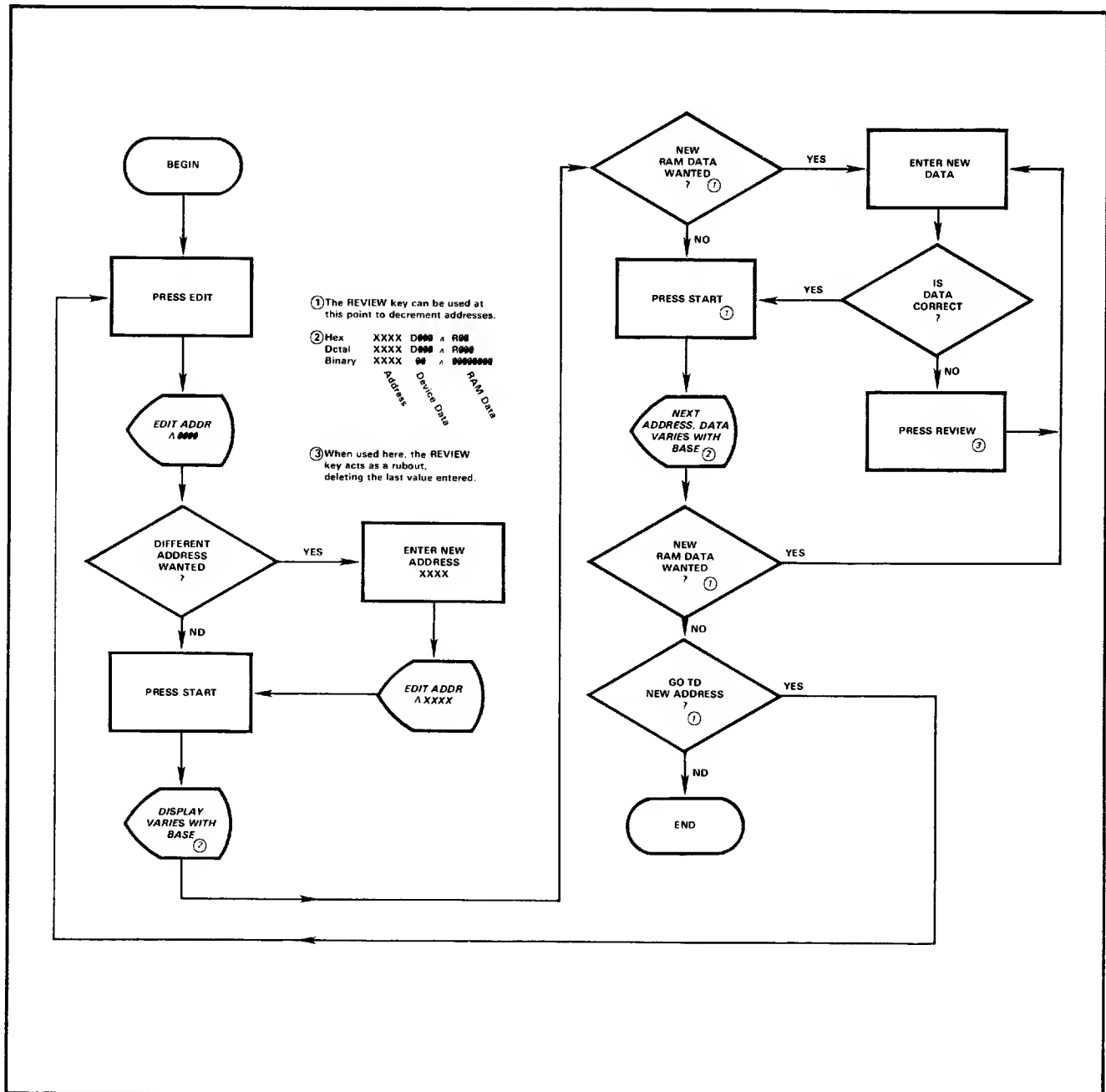


Figure 3-10. Edit

### 3.5 THE SELECT KEY

The SELECT key gives you access to additional functions that are used for changing the default values of parameters, RAM data manipulations, and accessing certain less frequently used operations. These operations are select functions.

#### 3.5.1 ACCESSING SELECT FUNCTIONS

There are three ways to access Select Functions:

- Direct Entry
- Stepping, or
- Scrolling

In direct entry, press SELECT. The 22A will display "SELECT CODE ". Enter the hex code for the desired function or data translation format. The display will prompt you if any additional entries are required.

Repeated depressions of the SELECT key allow you to step through the complete menu of select functions. When the select function you want is displayed, initiate the operation by pressing START. To step backwards through the select functions, press the REVIEW key. The functions are displayed in hexadecimal order.

The 22A will also scroll through the whole select function menu automatically. This is done by pressing SELECT and then START. Each function is momentarily displayed before the programmer moves on to the next function. When the desired function is displayed, you can stop the menu by pressing any key. To back up, press REVIEW. Once the select function you want is displayed, initiate the operation by pressing START. The SELECT and REVIEW keys can also be used to scroll through options available on some select functions.

#### 3.5.2 DESCRIPTIONS AND KEY SEQUENCES

Table 3-2 lists the select functions, descriptions, and key sequences. The key sequences are for direct entry. When stepping or scrolling, simply skip the first two or three steps and enter the operation at the location designated with a pound (#) sign. The programmer signals that the operation is complete when two asterisks appear in the far right hand side of the display.

#### 3.5.3 POWER DOWN SAVE FEATURE

Select function FE is the 22A's Power Down Save feature. This allows you to select and save, for future use, commonly set parameter values. These operating parameters are themselves select functions (except family and pinout codes). Parameters which can be Power Down Saved are listed in table 3-1.

When you first receive your programmer, a default is in effect for each of these parameters until you change it. The select function code, name and original default value are listed in table 3-1.

Table 3-1. Power Down Save Parameters and Original Default States

CODE	SELECT FUNCTION DISPLAY NAME	ORIGINAL DEFAULT STATE
B3	FORMAT NUMBER	50 ASCII-Hex (Space)
DA	BAUD RATE	9600
DB	PARITY	None
DC	STOP BITS	One
D8	RECORD SIZE	16 bytes
D9	NULLS	One
F1	REMOTE MODE	Remote Mode off
F4	NIBBLE MODE	Byte mode
FB	PORT EN/DIS	Disabled
FC	REMOTE ON OFF	00 00 (Disabled)
FD	UV TIMEOUT	35 minutes
F5, F6 or F7	RADIX (number base)	Hexadecimal
F9	TIMEOUT	On
--	Family & Pinout Codes	Family: 35 Pinout: 33

The proper procedure for performing a Power Down Save is:

1. Change any parameter value(s) by executing the appropriate select function(s), according to the instructions in table 3-2.
2. Execute select function FE (Power Down Save) according to the instructions in table 3-2.

### 3.6 ERASING YOUR MOS PROMS

The 22A provides you with the capability of erasing programmed MOS EPROMS. The programmer's built-in ultraviolet (UV) lamp can erase any programmed MOS EPROM listed in table 1-1.

#### 3.6.1 UV LAMP SPECIFICATION

The UV lamp intensity is rated at 7000 uwatt/cm<sup>2</sup>. Typically, EPROM device manufacturer's recommend an erasure dose of 15 watt-seconds/cm<sup>2</sup>. This yields an erasure time of 35 minutes.

#### 3.6.2 PROCEDURE FOR ERASING MOS PROMS

The following step-by-step procedure explains how to erase MOS EPROMS.

1. Open the UV Lamp cover door. See figure 3-11.
2. Place the MOS EPROMS you wish to erase on top of the UV tube with the PROM pins up. See figure 3-11.

Table 3-2. Select Functions

CODE	MENU DISPLAY		DESCRIPTION	KEY SEQUENCE	ENTRY	DISPLAY
<b>DATA MANIPULATION COMMANDS</b>						
A1	SWAP NIBBLES	A1	Exchanges high and low order nibbles of every byte.	1. Press SELECT. 2. Enter A1. #3. Press START to exchange high or low order nibbles of every byte.	SWAP NIBBLES SWAP NIBBLES	A1 **
A2	FILL RAM	A2	Fills RAM from the last EDIT address to the end of RAM with variable hex data. The default data value is 00. If Select Function F4 has been specified, it will fill only the lower order nibble of RAM; otherwise it will default to the word width.	1. Press SELECT. 2. Enter A2. #3. Enter the hex data (XX). 4. Press START.	FILL RAM 00 FILL RAM XX FILL RAM	A2 A2 **
A3	INVERT RAM	A3	Performs the ones complement of 4 or 8 bits of each word as determined by the word size in effect.	1. Press SELECT. 2. Enter A3. #3. Press START to complement all of RAM.	INVERT RAM INVERT RAM	A3 **
A4	CLEAR ALL RAM	A4	Clears all of RAM to zeros.	1. Press SELECT. 2. Enter A4. #3. Press START.	CLEAR ALL RAM CLEAR ALL RAM	A4 **
A5	SPLIT RAM	A5	Splits odd- and even-addressed bytes in RAM about a center point, dividing them into two adjacent blocks occupying the same original amount of RAM. The center point must be a power of two between 0 and the RAM midpoint. The default center point is the RAM midpoint (XXXX).	1. Press SELECT. 2. Enter A5. #3. Enter the center point (YYYY). 4. Press START to split RAM.	SPLIT RAM ^ SPLIT RAM ^ SPLIT RAM	XXXX YYYY **
A6	SHUFFLE RAM	A6	Shuffles the block of RAM addresses immediately above the center point with the block below, placing the lower-block bytes at even-numbered addresses starting with 0 and the upper-block addresses at odd-numbered addresses starting with 1. The center point must be a power of two between 0 and the RAM midpoint. The default center point is the RAM midpoint (XXXX).	1. Press SELECT. 2. Enter A6. #3. Enter the center point (YYYY) if the default is not correct. 4. Press START to shuffle RAM.	SHUFFLE RAM SHUFFLE RAM SHUFFLE RAM	XXXX YYYY **
<b>UTILITY AND INQUIRY COMMANDS</b>						
B0	DEVICE SIZE	B0	Displays the device word size and word width.	1. Press SELECT. 2. Enter B0.	DEV SZ XXXX Y device size L word width	**

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number have been displayed. This action initiates the operation.



Table 3-2. Select Functions (continued)

CODE	MENU DISPLAY	ENTRY	DESCRIPTION	KEY SEQUENCE	DISPLAY
B1	<i>SUMCHECK RAM B1</i>		Displays the RAM sum-check.	1. Press SELECT. 2. Enter B1.	<i>SUMCHECK XXXX</i> **
B2	<i>SYSTEM CONFIG B2</i>		Displays the software configuration number, RAM size, model number and software version number.	1. Press SELECT. 2. Enter B2.	<i>XXXX YYK 22A VO1</i> <i>Configuration RAM Size Model Number Software Version</i>
B3	<i>FORMAT NUMBER B3</i>		Displays the data translation format in effect and allows you to change it. The default value is ASCII-Hex (Space), 50, or the previously stored format.	1. To see the data translation format in effect: a. Press SELECT. b. Enter B3. + #c. If a new format is desired, enter the format code (XXX). d. Press START. e. Press START. 2. To enter the format code directly: a. Press SELECT. b. Enter the format number (XXX). c. Press START. + d. Press START.	<i>HEX SPCE STX</i>  <i>FORMAT NO XXX</i> <i>FORMAT NAME</i> <i>FORMAT NO XXX</i> **  <i>SELECT CODE</i>  <i>FORMAT NO XXX</i> <i>Format Name</i> <i>FORMAT NO XXX</i> **
B9	<i>DISPLAY TEST B9</i>		Lights all display segments for 4 seconds.	1. Press SELECT. 2. Enter B9. #3. Press START to test.	<i>DISPLAY TEST</i> <i>B9</i> <i>DISPLAY TEST</i> <i>XX</i>
C1	<i>CALIBRATION C1</i>		Puts the programmer in the calibration mode. This function is inhibited in remote operation. See Section 4, Calibration.	1. Press SELECT. 2. Enter C1. #3. Press START to execute calibration Step 1 (or increment step number). 4. To jump forward to an advanced calibration step, enter the desired step number and press START. 5. To decrement calibration step number, press REVIEW.	<i>CAL STEP 01</i>

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number was displayed. This action initiates the operation.

+ Pressing SELECT instead of START at this point will step you through the format menu.

Table 3-2. Select Functions (continued)

CODE	MENU DISPLAY		DESCRIPTION	KEY SEQUENCE	ENTRY DISPLAY	
CC	DSP FAM/PIN	CC	Displays the family and pinout selected or the equivalent family and pinout code for device's that have built-in electronic identifiers.	1. Press SELECT. 2. Enter CC. 3. Press START.	DSP FAM/PIN CC FF PP	**
CD	VIEW ID	CD	Displays the device's electronic identifier one byte at a time.	1. Press SELECT. 2. Enter CD. 3. Press START to increment through the 16-bytes of ID code.	VIEW ID CD 0000 XX	
CE	NORMAL REJECT	CE	Selects the Commercial reject count for the number of program pulses.	1. Press SELECT. 2. Enter CE. #3. Press START.	NORMAL REJECT NORMAL REJECT	CE **
CF	ONE PULSE REJ	CF	Sets single pulse reject count.	1. Press SELECT. 2. Enter CF. #3. Press START.	ONE PULSE REJ ONE PULSE REJ	CF **
F0	PROGRAM COUNT F0		Displays the number of devices programmed since power-up or last reset.	1. Press SELECT. 2. Enter F0. #3. Press START if you want to reset the parts count to 00.	PROGRAM COUNT PROGRAM COUNT	XX **
F1	REMOTE MODE	F1	Puts the programmer in Computer Remote Control.  If in computer remote control you were to execute a power down save operation, control would be from the remote source the next time the machine was powered-up. Exiting the remote mode returns control of the programmer to the front panel keyboard.	1. Press SELECT. 2. Enter F1. #3. Press START to enter the remote mode.	REMOTE MODE REMOTE MODE	F1 ☐
F3	LOCK DATA ON	F3	Sets the data lock on. This protects the the data in RAM for a series of identical programming operations. While the data lock is in effect, keys used to manipulate data are disabled. The only operations possible are: • Copy operations that move data from RAM to the port or device • Verify operations • Abort operation in progress • Release data lock	1. To engage data lock: a. Press SELECT. b. Enter F3. c. Press START.  2. To release data lock: a. Press SELECT. b. Press PORT. c. Press REVIEW. The data lock is now inactive.	LOCK DATA ON LOCK DATA ON  PASSWORD? SELECT CODE A	      **

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number have been displayed. This action initiates the operation.

Table 3-2. Select Functions (continued)

CODE	MENU DISPLAY		DESCRIPTION	ENTRY KEY SEQUENCE	DISPLAY	
F4	NIBBLE MODE	F4	Selects a 4-bit word size to override 8-bit programming, or for I/O transfers.	1. Press SELECT. 2. Enter F4. #3. Press START.	NIBBLE MODE NIBBLE MODE	F4 **
F5	BINARY BASE	F5	Sets the number base for Edit operations to binary.	1. Press SELECT. 2. Enter F5. #3. Press START to enable binary base for Edit operations.	BINARY BASE BINARY BASE	F5 **
F6	OCTAL BASE	F6	Sets the number base for Edit operations to octal.	1. Press SELECT. 2. Enter F6. #3. Press START to enable octal base for Edit operations.	OCTAL BASE OCTAL BASE	F6 **
F7	HEX BASE	F7	Resets the number base for Edit operations to hex. This is the default base.	1. Press SELECT. 2. Enter F7. #3. Press START to enable hex base.	HEX BASE HEX BASE	F7 **
F8	BYTE/NIB MODE	F8	Nullifies select function F4; allows word size of the device selected to take effect.	1. Press START. 2. Enter F8. #3. Press START to establish the word size of the selected device.	BYTE/NIB MODE BYTE/NIB MODE	F8 **
FD	UV TIMEOUT	FD	Sets the UV lamps erasure time for programmed EPROMS. The erasure time range is 1-99 minutes.	1. Press SELECT. 2. Enter FD. #3. Enter the erasure time (YY). 4. Press START.	UV TIMEOUT XX UV TIMEOUT YY UV TIMEOUT	FD FD **
FE	POWER DOWN SAVE	FE	Allows you to save the values currently in effect for the following functions: • Data Translation Format • Record Size • Radix (Number base) • Nulls • Stop Bits • Parity • Baud Rate • I/O Timeout Status • UV Timeout • Family and Pinout Codes • Port Enable/Disable Status • Remote ON/OFF • Computer Remote Mode* • Nibble Mode	1. Press SELECT. 2. Enter FE #3. Press START.	POWER DOWN SAVE POWER DOWN SAVE	FE **

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number was displayed. This action initiates the operation.

\* When executing a power down save in Computer Remote Control, all of the preceding values are saved except data translation format and number of nulls. In both cases, the defaults (Data Format 81 and no nulls) will be in effect.

Table 3-2. Select Functions (continued)

CODE	MENU DISPLAY	DESCRIPTION	KEY SEQUENCE	ENTRY	DISPLAY
<b>SERIAL I/O COMMANDS</b>					
D7	LEADER OUTPUT D7	Sends 50 nulls from the serial port.	1. Press SELECT 2. Enter D7 #3. Press START to output a 50-null leader.	LEADER OUTPUT LEADER OUTPUT	D7 **
D8	SIZE RECORD D8	Changes the number of bytes per data record on the serial output. The value entered must be in hex notation.	1. Press SELECT. 2. Enter D8. The record size in effect (XX) will be displayed. 3. If a new value is desired enter it (YY). 4. Press START.	SIZE REC XX SIZE REC YY SIZE RECORD	D8 D8 **
D9	NULL COUNT D9	Sets up to 254 nulls (FE in hexadecimal) following each data record on output. Selecting 255 (FF) sends no nulls and no line feed. Default is 1 null.	1. Press SELECT. 2. Enter D9. The number of nulls in effect will be displayed. 3. If a different value is wanted, enter the hexadecimal value (XX). 4. Press START to enable the new null count.	NULL COUNT NULL COUNT NULL COUNT	01 D9 XX D9 **
DA	BAUD RATE DA	Allows you to select the programmer's baud rate. Available baud rate selections are: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 and 19200.	1. Press SELECT. 2. Enter DA. #3. By pressing the SELECT or REVIEW key, scroll to the desired baud rate. 4. Press START.	BAUD RATE XXXXX BAUD RATE	DA **
DB	PARITY DB	Allows you to select the programmer's parity setting. Parity settings are: none, odd or even.	1. Press SELECT. 2. Enter DB. #3. Press SELECT until the desired parity setting appears in the display. 4. Press START.	PARITY XXXX PARITY	DB **

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number have been displayed. This action initiates the operation.

Table 3-2. Select Functions (continued)

CODE	MENU DISPLAY	ENTRY	DESCRIPTION	KEY SEQUENCE	DISPLAY
DC	STOP BITS	DC	Allows you to select either one or two stop bits.	1. Press SELECT. 2. Enter DC. #3. Press SELECT until appropriate number of stop bit(s) appear. 4. Press START.	STOP BITS XXX DC STOP BITS **
F9	TIMEOUT	F9	Selects the standard 25-second I/O timeout. Selecting a "yes" display means the timeout is "on". Selecting a "no" display means the timeout is disabled.	1. Press SELECT. 2. Enter F9. #3. Press SELECT until the desired setting appears (i.e. yes or no). 4. Press START to place the selected state in effect.	TIMEOUT YES F9 TIMEOUT **
FA	CHAR OUTPUT	FA	After this code is entered, enter the hex code for an ASCII character (see Appendix B). The character is transmitted to the port each time you press START. This function is inhibited in remote control.	1. Press SELECT. 2. Enter FA. #3. Enter hex value of ASCII character. 4. Press START. 5. Repeat step 4 to repeat the character. Repeat steps 3 and 4 to select other characters.	CHAR OUTPUT 00 CHAR OUTPUT XX CHAR OUTPUT ^XX CHAR OUTPUT ^XX
FB	PORT EN/DIS	FB	Enables Standard Remote Control and the Input Interrupt and forces the RTS line high at all times for remote control from peripherals requiring hardware handshake. The default at power-up is RTS low and Remote Control and Interrupt disabled.	1. Press SELECT. 2. Enter FB. #3. Press SELECT until the appropriate port setting appears in the display. 4. Press START to put this port setting into effect.	PORT EN/DIS FB PORT EN/DIS **
FC	REMOTE ON OFF	FC	Allows you to turn remote control on and off remotely via hexadecimal codes you select. (Applies to both standard and Optional Computer Remote Control.) See Appendix D for a more detailed description.	1. Press SELECT. 2. Enter FC. #3. Enter on code XX; Press START. 4. Enter off code YY. 5. Press START.	RMT ON OFF 00 00 RMT ON OFF XX 00 RMT ON OFF XXYY RMT ON OFF **

#Entry point when scrolling or stepping through the menu. Make sure you have pressed START after the function name and number have been displayed. This action initiates the operation.

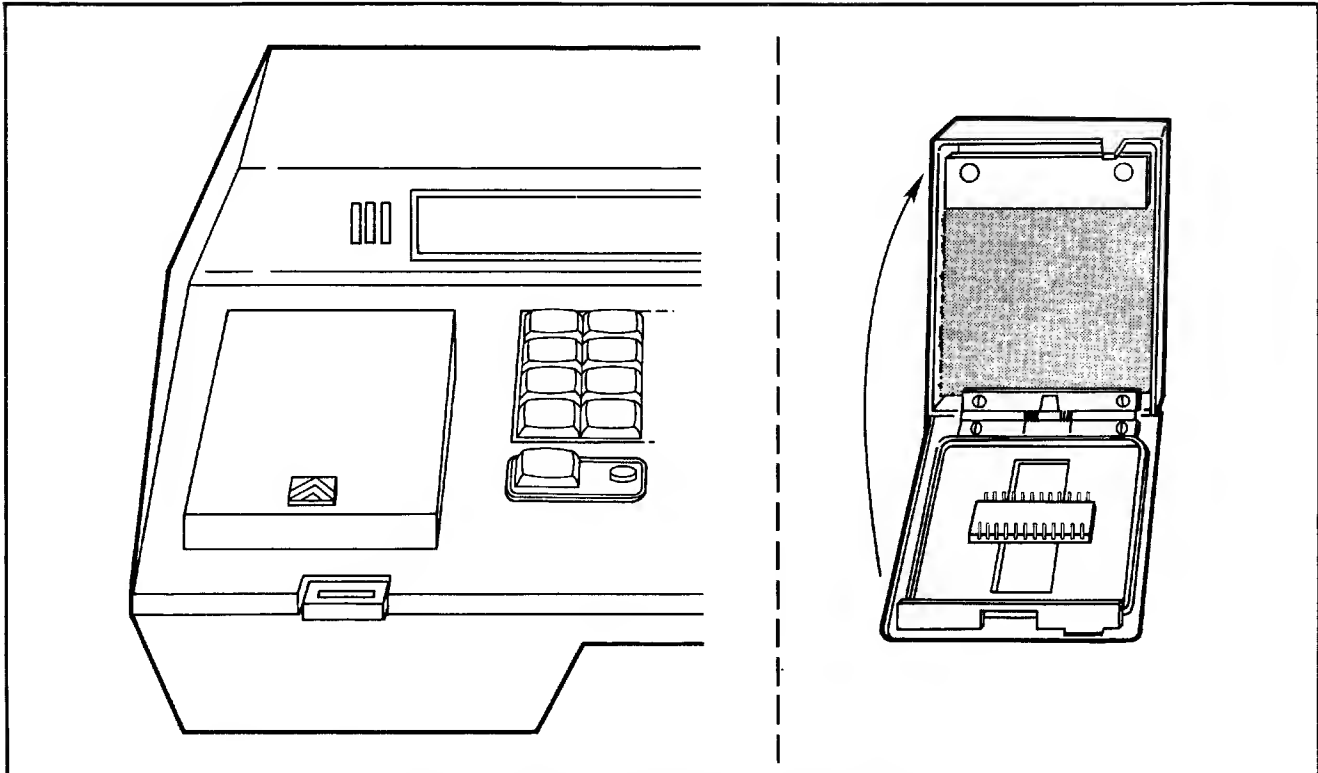


Figure 3-11. Opening the UV Lamp Cover Door

3. Select the appropriate erasure time according to the PROM manufacturer's specifications. The programmer defaults to 35 minutes. Go to step 5 if you have already set the UV timeout (or if the default timeout is being used.)
4. Enter the time value chosen by executing select function FD (UV Timer Set). Refer to table 3-2.
5. Close the UV lamp cover door.
6. Press the UV key located on the programmer's front panel. The UV LED is lit and the PROMs are in the selected erasure cycle.

**NOTE**

1. The serial paper tape reader cannot be used while the UV lamp is activated.
  2. At this point in the procedure, pressing the UV key while the lamp is on causes the programmer to reset itself to the original UV timeout selected.
  3. UV lamp on time is lengthened in conjunction with other machine operations.
7. When the UV timeout expires, the UV LED turns off. Your MOS PROMs are now erased.
  8. Open the UV lamp cover door and remove your PROMs.

**CAUTION**

The UV lamp cover door closes on an interlock switch. If the door is opened during the erase cycle, the UV lamp will automatically switch off preventing any possible UV lamp radiation exposure. **DO NOT DEFEAT THE OPERATION OF THIS INTERLOCK SWITCH. EXPOSURE TO UV LAMP RADIATION IS DANGEROUS TO EYES AND SKIN.**

### 3.7 SOURCE/DESTINATION METHOD OF SYNTAX

The 22A uses a source/destination method of syntax when operations are executed with the COPY and VERIFY keys.

The COPY and VERIFY function keys tell the programmer whether the data is to be copied from one medium to another or verified against other data to ensure they are identical. These keys initiate the operation and are used in conjunction with the source/destination keys (PORT, RAM and DEVICE).

The operator initiates the operation by choosing either the COPY or VERIFY key and then specifies the source of data (PORT, RAM or DEVICE) and then the destination for that data (again, either PORT, RAM or DEVICE). By using table 3-3, you can determine, based on the source/destination concept, the operation you wish to

execute. This table also provides you with the operational flowchart's figure location within this manual.

When the COPY key is used, data is moved from the source to the destination; for example, from the programmer data RAM to a blank device in the socket. At the completion of this operation the device will contain a copy of the data in the programmer data RAM-the device is now "programmed."

When the VERIFY key is used, the programmer makes a byte-by-byte comparison of the data in RAM with the data in a programmed device or input from the serial port. In a Verify operation, data in two mediums is compared, rather than transferred.

### 3.7.1 GENERALIZED KEY SEQUENCE SYNTAX

The generalized key sequence syntax for the COPY and VERIFY function keys is:

[function] [source] XXXX/YYYY [destination] ZZZZ [START]

XXXX, YYYY, and ZZZZ are parameters associated with the source/destination keys. XXXX is the beginning source address. YYYY is the source block size and ZZZZ is the beginning destination address. Table 3-4 provides the usage, definition, and default values for these parameters. If the default values are correct, it is not necessary to enter them in the key sequences for the operation.

Table 3-3. COPY and VERIFY keyboard Operations

COPY KEY				
DESTINATION SOURCE	DEVICE (blank device)	RAM (programmer data RAM)	PORT (peripheral)	
DEVICE (master device)		LOAD FROM DEVICE See Figure 3-3		
RAM (programmer data RAM)	PROGRAM DEVICE See Figure 3-5	BLOCK MOVE See Figure 3-7	OUTPUT TO PORT See Figure 3-6	
PORT (peripheral)		INPUT FROM PORT See Figure 3-4		

VERIFY KEY				
DESTINATION SOURCE	DEVICE (previously programmed device)	RAM (programmer data RAM)	PORT (peripheral)	
DEVICE (master device)		VERIFY DEVICE See figure 3-8		
RAM (programmer data RAM)	VERIFY DEVICE See Figure 3-8		INPUT VERIFY See Figure 3-9	
PORT (peripheral)		INPUT VERIFY See Figure 3-9		


 Illegal Source/Destination Combination

Table 3-4. Address Parameters

KEY	DENOTED BY	ADDRESS PARAMETER	DEFINITION AND DEFAULT
DEVICE	XXXX or ZZZZ	Begin Device Address	First device address from which data is output or to which data is input. The default is 0. To return to the default value press the REVIEW key or enter 0.
RAM	XXXX or ZZZZ	Begin RAM Address	First data RAM address from which data is output or to which data is input. The default is 0. To return to the default value press the REVIEW key or enter 0.
PORT	XXXX or ZZZZ (6 or 8 digits for 16-bit translation Formats)	Address Offset	When addresses larger than RAM are to be dealt with, the address offset is subtracted from all addresses on input and added on output. The result is added to the Begin RAM Address. The default is 0 on output and the first incoming address on input. If you change the Address Offset and want to return to the default, enter FFFF. This will return you to the default.
DEVICE RAM PORT	YYYY	Block Size	The number of bytes to be transferred. The default value is the device size in device-related operations. In port-related operations it is from the first RAM address specified to the end of RAM. To return to the default value, press REVIEW or enter 0.
*Whenever defaults are in effect ADDR is displayed for address parameters and SIZE is displayed for Block Size.			

### 3.8 STANDARD REMOTE CONTROL

The 22A's Standard Remote Control capability allows control of the programmer's operations from a terminal. Your 22A also features computer remote control which is described in Appendix C.

#### NOTE

*To allow operation of the 22A in Standard Remote Control, Select Function FB must be set to the Port enable mode. As long as the controlling instrument is properly interfaced (see Section 2, Installation), all operations can be done either on the programmer keyboard or the controlling instrument.*

Table 3.5. Command Entry in Remote Control

KEYBOARD COMMAND	REMOTE CONTROL COMMAND
COPY	CO <sub>v</sub>
VERIFY	VE <sub>v</sub>
PORT	PO <sub>v</sub>
RAM	RA <sub>v</sub>
DEVICE	DE <sub>v</sub>
SELECT	SE <sub>v</sub>
REVIEW	/
EDIT	ED <sub>v</sub>

#### 3.8.1 COMMAND PROTOCOL

The syntax for Remote Control is similar to that of keyboard operations, using the source/destination syntax method.

When keying in commands from a terminal, the 22A recognizes the first two characters of each command (except REVIEW), as shown in table 3-5.



The space bar (denoted by v) used after the command acts as a delimiter, setting the boundaries for that command. The programmer will not define the characters input until the space bar is used. And since the programmer only recognizes the first two characters, some variation is possible. For example:

COvDEvXXXvYYYYvTOvRAvZZZ[CR]

COPYvDEVICEvXXXvYYYYvTOvRAMvZZZ[CR]

In the examples above, the programmer will load the data in the device into the programmer RAM, in the same way as a Load from Device is done from the keyboard.

The carriage return [CR] at the end of the line acts as an execute key. As characters are input to the programmer, they are stored until the [CR] is input, signalling the programmer to execute that line of characters.

#### NOTE

*The word "TO" must be keyed in prior to the destination.*

### 3.8.2 COMMAND ENTRY

There are two methods of command entry, direct or interactive.

In direct command entry, you type in the commands, using the space bar between words, as shown in the examples in paragraph 3.8.1. X, Y, and Z values are optional.

The interactive method streamlines the entries required of the operator. In the interactive method, you key in the function, then press [CR]. The terminal displays prompt you just as the 22A keyboard does with, for example, COPY DATA FROM V if the COPY key is used. The operation occurs just as it does when using the programmer's keyboard except that you key in commands rather than pressing keys on the 22A.

When entering data on the terminal, the slash (/) is used in place of the REVIEW key. When pressed, it will delete the previous character or characters. It will not delete anything prior to a space.

### 3.8.3 INPUTTING PARAMETERS

The parameters required are the same as those given in table 3-4 for keyboard operations. The values entered must be valid 4-digit hexadecimal values. When the default value is satisfactory, no new value needs to be entered. If it is necessary to skip over the source address (when its default is correct) and change the block size, input a comma (,) or the space bar. Figure 3-12 shows examples of inputting parameters.

#### WHEN DEFAULT VALUES ARE ALL CORRECT:

##### DIRECT ENTRY

COvDEvTOvRA[CR]

##### INTERACTIVE

CO[CR]

(COPY DATA FROM > displayed on terminal)

DE[CR]

(DEV ADDR,SIZE > displayed on terminal)

TOvRA[CR]

(CO DEV > RAM ADDR > displayed on terminal)

#### NOTE

*The commands shown here are examples only. The complete list of commands is in Table 3-6.*

#### WHEN NO DEFAULT VALUES ARE CORRECT:

##### DIRECT ENTRY

COvDEvXXXvYYYYvTOvRAvZZZ[CR]

##### INTERACTIVE

CO[CR]

(COPY DATA FROM > displayed on terminal)

DE[CR]

(DEV ADDR,SIZE > displayed on terminal)

XXXvYYYvTOvRA[CR]

(COPY DEV > RAM ADDR > displayed on terminal)

ZZZ[CR]

#### WHEN SOURCE ADDRESS DEFAULT IS CORRECT AND BLOCK SIZE DEFAULT IS INCORRECT:

##### DIRECT ENTRY

COvDEV, XXXvTOvRA[CR]

##### INTERACTIVE

CO[CR]

(COPY DATA FROM > displayed on terminal)

DE[CR]

(DEV ADDR,SIZE > displayed on terminal)

,YYYvTOvRA[CR]

(COPY DEV > RAM ADDR > displayed on terminal)[CR]

Figure 3-12. Inputting Remote Control Parameters

### 3.8.4 COPY AND VERIFY OPERATIONS

Table 3-6 lists the basic Remote Control protocols for Copy and Verify operations. Each is a "worst case" example, showing entry of all parameters. These will not be necessary when the default values are satisfactory.

### 3.8.5 EDIT OPERATIONS

There are three variations to Remote Control Edit operations.

- To view the last address edited (the default is 0), key in:

ED[CR]

- To view a specific address, key in:

EDvHHHH[CR]


desired address

Table 3-6. Remote Control Commands

OPERATION	DIRECT ENTRY	ENTRY	INTERACTIVE ENTRY TERMINAL DISPLAY
Input from Port	COvPOvXXXX*vYYYYvTOvRAvZZZ- + [CR]	CO[CR] PO[CR] XXXX, YYYYvTOvRA[CR] ZZZ[CR]	COPY DATA FROM > POR ADDR, SIZE > COPY POR>RAM ADDR > ZZZ[CR]
Load from Device	COvDEvXXXXvYYYYvTOvRAvZZZ + [CR]	CO[CR] DE[CR] XXXX, YYYYvTOvRA[CR] ZZZ[CR] + FF PP	COPY DATA FROM > DEV ADDR, SIZE > COPY DEV > RAM ADDR > ZZZ[CR]
Program Device	COvRAvXXXXvYYYYvTOvDEvZZZ + [CR]	CO[CR] RA[CR] XXXX, YYYYvTOvDE[CR] ZZZ[CR] + FF PP	COPY DATA FROM > RAM ADDR, SIZE > COPY RAM > DEV ADDR > ZZZ[CR]
Output to Port	COvRAvXXXXvYYYYvTOvPOvZZZ* + [CR]	CO[CR] RA[CR] XXXX, YYYYvTOvPO[CR] ZZZ[CR]	COPY DATA FROM > RAM ADDR, SIZE > COPY RAM > POR ADDR > ZZZ[CR]
Block Move	COvRAvXXXXvYYYYvTOvRAvZZZ + [CR]	CO[CR] RA[CR] XXXX, YYYYvTOvRA[CR] ZZZ[CR]	COPY DATA FROM > RAM ADDR, SIZE > COPY RAM > RAM ADDR > ZZZ[CR]
Verify Device	VEvRAXXXvYYYYvTOvDEvZZZ + [CR]	VE[CR] RA[CR] XXXX, YYYYvTOvDE[CR] ZZZ[CR] + FF PP	VERIFY DATA FROM > RAM ADDR, SIZE > VE RAM > DEV ADDR > ZZZ[CR]
Input Verify	VEvRAvXXXXvYYYYvTOvPOvZZZ* + [CR]	VE[CR] RA[CR] XXXX, YYYYvTOvPO[CR] ZZZ[CR]	VERIFY DATA FROM > RAM ADDR, SIZE > VE RAM > POR ADDR > ZZZ[CR]

+ Enter Family and Pinout Codes.  
 \* I/O offset address XXXX or ZZZZ is six or 8 digits if 16-bit data translation format is in effect.

- To enter at a specific address, enter:

EDvHHHHvHH[CR]  
  
 desired address      data\*

*\*The exact number of digits will vary depending on the base specified.*

Just as in keyboard Edit operations, Remote Control Edit operations take into account any previously set device address parameters.

### 3.8.6 SELECT FUNCTIONS

In Remote Control it is possible to display the whole Select Function menu at one time. This is done by entering:

SE[CR]

Figure 3-13 shows the Select Function menu.

Individual Select Functions can be accessed in two ways.

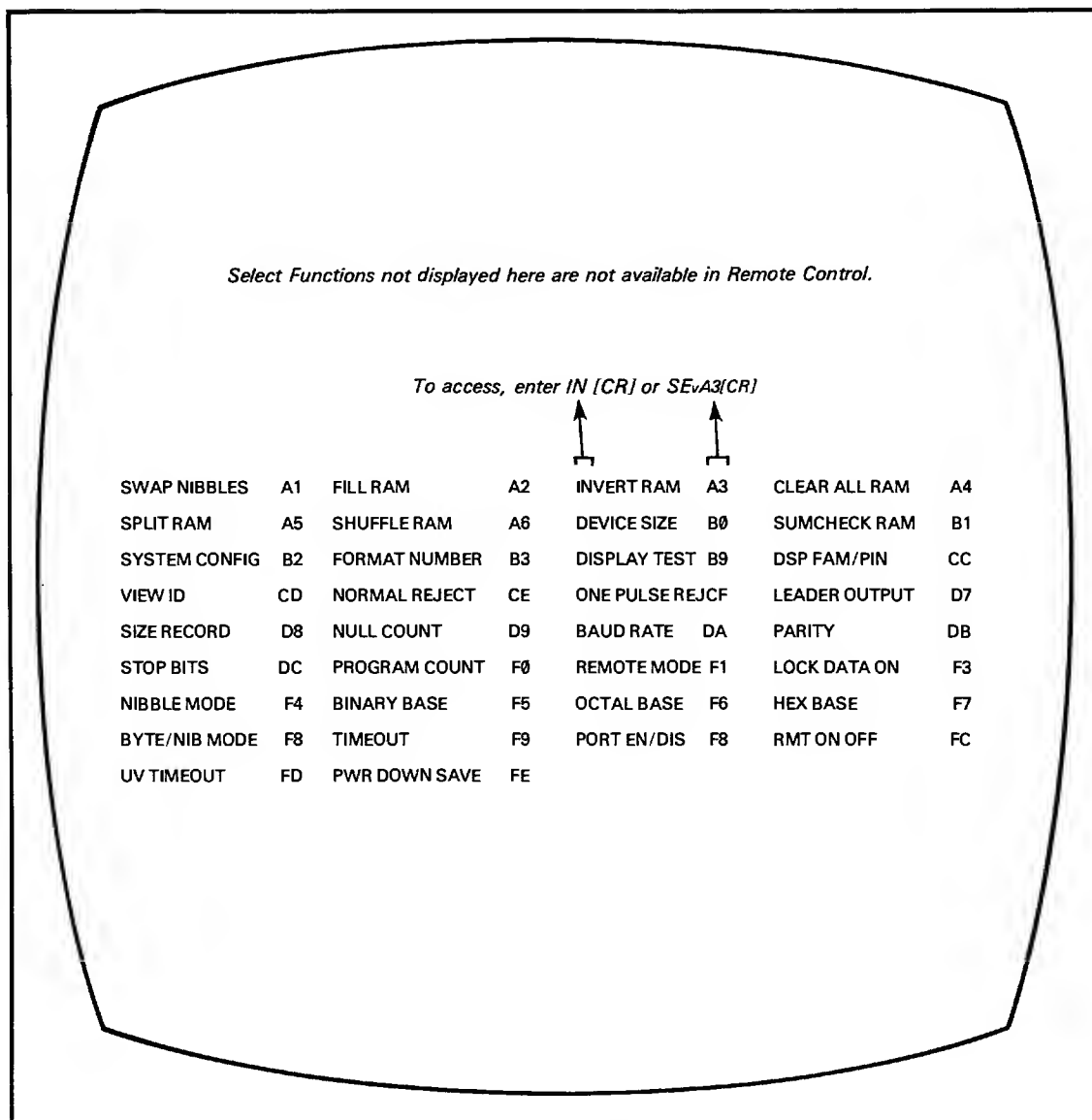


Figure 3-13. Select Function Menu in Remote Control

- Entering the first two letters of the Select Function (as shown in Figure 3-13) followed by a [CR].
- Entering SEvHH[CR] where HH is the hex code for the desired Select Function (when no additional parameters are required), or entering SEvHHvXXXX[CR] when XXXX is a parameter required for that Select Function.

To view the default values in effect for a specific Select Function, enter SEvHH[CR]. This will display the value in effect.

To view the entire data translation format menu: enter either the first two letters, FO, followed by a [CR] or SEvB3[CR]. The entire menu and the format currently in effect will be displayed as in Figure 3-14.

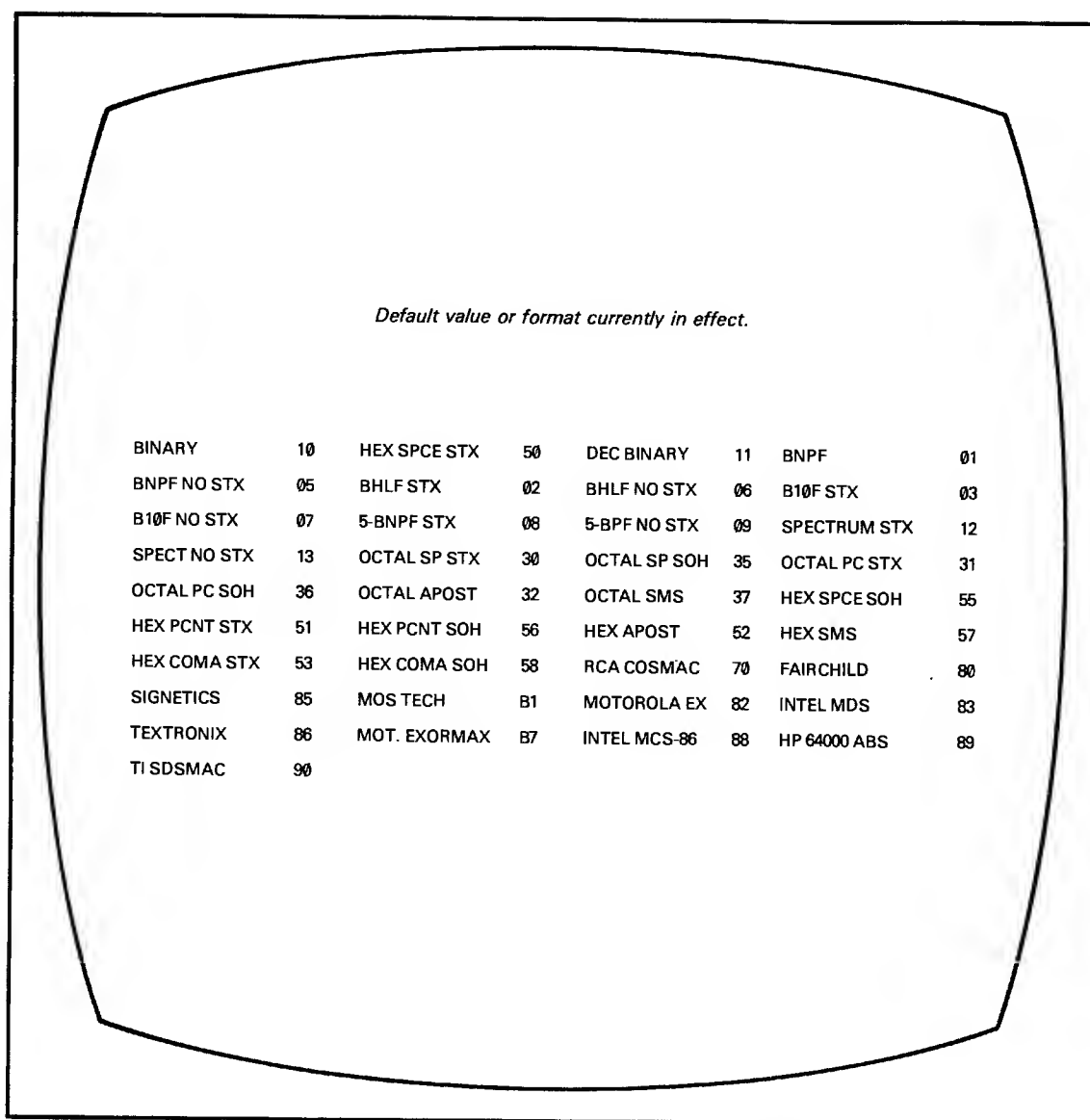


Figure 3-14. Data Translation Format Menu in Remote Control

#### NOTE

The following Select Functions can be viewed in Standard Remote Control, but cannot be changed:

- Baud Rate DA
- Parity DB
- Stop Bits DC
- Port Enable FB
- Timeout F9

### 3.9 ERROR CODES

Table 3-7 gives descriptions and corrective actions for the 22A's error codes.

**Table 3-7. Error Codes**

DISPLAY		DESCRIPTION	CORRECTIVE ACTION
<i>NO ID FOUND</i>	<i>A1</i>	Programmer failed to detect an electronic identifier in the device.	Enter the correct family and pinout code for the device. This information is listed in table 1-1.
<i>INVALID ID</i>	<i>A2</i>	Device cannot be programmed with the current family and pinout codes in effect.	Consult table 1-1 for the correct family and pinout codes for the device and reenter this information into the programmer.
<i>SORC/DEST ERR</i>	<i>15</i>	Illegal source/destination key sequence was entered.	Check key sequence and re-enter.
<i>COMMAND ERROR</i>	<i>17</i>	Illegal key sequence while in Standard Remote Control.	Check key sequence and re-enter.
<i>NONBLANK</i>	<i>20</i>	Device failed the blank test.	Press START and try to program the device. It will abort if the nonblank bits prevent programming.
<i>ILLEGAL BIT</i>	<i>21</i>	Not possible to program the device due to already programmed locations of incorrect polarity.	Erase the device if possible or discard it.
<i>PROGRAM FAIL</i>	<i>22</i>	The program electronics were unable to program the device.	Either the device is bad or the programming module is inoperative or out of calibration.
<i>VERIFY FAIL 1</i>	<i>23</i>	The device data was incorrect on the first pass of the automatic verify sequence during device programming.	This error indicates that the device failed the low voltage verify; the data in the part is not the same as the RAM data.
<i>VERIFY FAIL 2</i>	<i>24</i>	The device was incorrect on the second pass of automatic verify sequence during programming.	This error indicates that the device failed the high voltage verify; data in the part is not the same as the RAM data.
<i>NO SOCKET ADP</i>	<i>25</i>	A device-related operation was attempted without any socket adapter installed.	Install the appropriate socket adapter. See table 1-3.
<i>WRONG SKT ADP</i>	<i>26</i>	Operation was attempted with the wrong socket adapter installed.	Install the appropriate socket adapter. See table 1-3.
<i>RAM EXCEEDED</i>	<i>27</i>	There is insufficient RAM to program the device; the total allotment of RAM resident is less than the word limit of the device.	Program smaller parts or buy enough extended RAM. If enough RAM is installed, it may be faulty.
<i>FAM/PIN ERROR</i>	<i>30</i>	An incorrect family and pinout code was entered from front panel control.	Check table 1-1 for the correct family and pinout codes for your device and reenter.
<i>EXCSS CURRENT</i>	<i>31</i>	In the operation just attempted, the device was drawing more current than the device manufacturer's specification.	If the device is faulty, replace it. If this is not the problem the fault may be with the programming electronics. Consult the troubleshooting information in Section 4.
<i>FAM/PIN ERROR</i>	<i>34</i>	An incorrect family and pinout code was entered from remote control.	Check table 1-1 for the correct family and pinout codes for you device and reenter.
<i>DEVICE ERROR</i>	<i>35</i>	Either an attempt was made to program a faulty device, or a program operation was attempted at an empty socket.	Replace the bad device or insert a device into the appropriate socket and then attempt a program operation.
<i>BAD CAL STEP</i>	<i>38</i>	An inappropriate calibration step was entered.	Recheck the measurement chart (see Section 4) for the correct calibration step and try again.
<i>FRAME ERROR</i>	<i>41</i>	The serial interface detected a start bit but the stop bit was incorrectly positioned.	Check the baud rate and stop bit setting.
<i>OVERRUN ERROR</i>	<i>42</i>	The serial interface received characters when the programmer was unable to service them.	Check the baud rate and stop bit setting.

Table 3-7. Error Codes (continued)

DISPLAY		DESCRIPTION	CORRECTIVE ACTION
<i>I/O TIMEOUT</i>	46	No character (or only nulls and rubouts) were received on serial input for 25 seconds after pressing the START key, or no characters could be transmitted for a period of 25 seconds due to the state of the handshake lines.	Check all connections; then restart operation.
<i>I/O OVERRUN</i>	48	The serial port input buffer received too many characters after the handshake line informed the sending device to stop.	Make sure the handshake lines are hooked up and operative.
<i>I/O VFY FAIL</i>	52	The data from the serial port did not match the data in RAM.	
<i>RAM WRITE ERR</i>	63	The programmer is unable to write the intended data in RAM.	Failure of the associated RAM chip; replace the failed chip.
<i>RAM DATA ERR</i>	64	The programmer detected a spurious change in RAM data.	Reload data into RAM. If problem persists, service the programmer or notify your local Data I/O Service Center.
<i>IRQ ERROR</i>	66	The IRQ line to the processor was held low for no apparent reason.	Ignore. If the error persists, service the programmer.
<i>NON-HEX CHAR</i>	67	Programmer received a non-hex character in Computer Remote Control.	Enter correct character.
<i>DATA LOCKED</i>	68	Data locked via Select Function F3.	Use the password to release data.
<i>PARITY ERROR</i>	81	The incoming data has incorrect parity.	Check the parity setting and try again.
<i>SUMCHECK ERR</i>	82	The sum-check field received by the programmer does not agree with its own calculated sum-check. For ASCII Binary formats, this error message indicates a missing F character.	Check all connections of units in the system, data format, and data source, and then try again.
<i>INVALID DATA</i>	84	The programmer received invalid or not enough data characters. Non-hex characters (formats 81-86)	Check the connection of all units in the system, data format and data source, and then try again.
<i>INVALID FORM</i>	90	Non-existent I/O format is selected in Computer Remote Control.	Enter a legal format code.
<i>I/O FORM ERR</i>	91	The programmer received an invalid character in the address field.	Check the connection of all units in the system, data format, and data source, and then try again.
<i>I/O FORM ERR</i>	92	The address check was in error. (Tektronix Hexadecimal format only.)	Check the connection of units in the system, data format, and data source, and then try again.
<i>I/O FORM ERR</i>	93	The number of input records did not equal the Record Count. (MOS Technology format only.)	Check the connection of all units in the system, data format, and data source, and then try again.
<i>BAD REC TYPE</i>	94	The record type was in error. (Intel-Intellec 8/MDS format only.)	Check the connection of all units in the system, data format, and data source, and then try again.
<i>BLOCK MOVE ERR</i>	97	Block Move was attempted outside RAM boundaries.	Redefine parameters.
<i>DEV EXCEEDED</i>	98	Programming data exceeded the last device address.	

## SECTION 4

# MAINTENANCE/ CALIBRATION/ TROUBLESHOOTING

### 4.1 OVERVIEW

The support material in this section has been provided to help you keep your 22A in optimum operating condition. General maintenance practices are discussed in section 4.2, and the basic troubleshooting procedures are described in section 4.4. For those 22A users who prefer to do their own calibration, detailed set up procedures, measurement charts and timing diagrams are provided in section 4.3 of this manual.

### 4.2 MAINTENANCE

Regular maintenance of the 22A consists of cleaning (section 4.2.1) and inspection (section 4.2.2).

#### 4.2.1 CLEANING

Inspect the 22A inside and out for accumulated dirt or dust. To gain access to the inside of the 22A, refer to section 4.3 and figure 4-1 for disassembly instructions. To clean the 22A:

1. Wipe any dust or dirt off the outside of the 22A with a clean, damp cloth.

#### NOTE

*Do not use abrasive cleaners or solvents.*

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

#### 4.2.2. INSPECTION

You can help prevent malfunctions by periodically inspecting your 22A. Check cable connections, circuit board and component mounting for shorts, opens, or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This situation, however, is an abnormal condition. If you cannot determine the cause of overheating, contact your nearest Data I/O Service Center.

### 4.3 CALIBRATION

The need for calibration varies with how much you use your 22A. Generally, we suggest calibration whenever:

- 1) programming yields fall below the manufacturer's recommended minimums, 2) troubleshooting has been completed, or 3) if the user's company policy requires periodic calibration certification.

Calibration of the 22A consists of two parts:

1. DC calibration—consists of measuring and adjusting critical DC voltage levels generated by the 22A (steps 1-20 on the measurement chart).

2. Waveform observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturer's critical voltage and timing specifications (steps 21-22 on the measurement chart).

The following equipment is required for calibrating the 22A:

- Three and a half digit, digital voltmeter (DVM)
- Dual trace oscilloscope (Tektronix 465 or equivalent)
- Potentiometer adjustment tool (tweaker), or 1/8" flat blade screwdriver.
- Resistors:
  - 20 ohm 2 watt
  - 100 ohm 1/4 watt
  - 100 ohm 2 watt (no wire wound)
  - 110 ohm 10 watt
  - 120 ohm 1/4 watt
  - 135 ohm 10 watt

#### NOTE

*All resistors should be within  $\pm 1\%$  of nominal value.*

To prepare your 22A for calibration, follow these procedures:

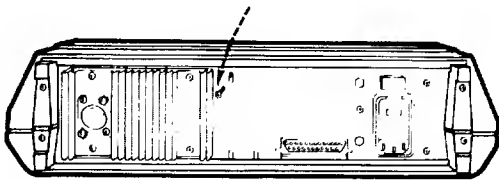
1. Turn the programmer power off; see section 3.3 for details.
2. Disassemble the 22A by referring to figure 4-1 and following these instructions:
  - a. Turn the programmer so that the rear panel faces you. Remove the screw located in the top-central portion of the panel.
  - b. Stand the programmer on end so that the bottom of the programmer faces you. The programmer's feet should be firmly planted on the table and the carrying handle should be pointing up.
  - c. Remove the 8 screws from the bottom of the programmer.

#### CAUTION

**During reassembly, do not overtighten these 8 screws (9.0 in-lb max).**

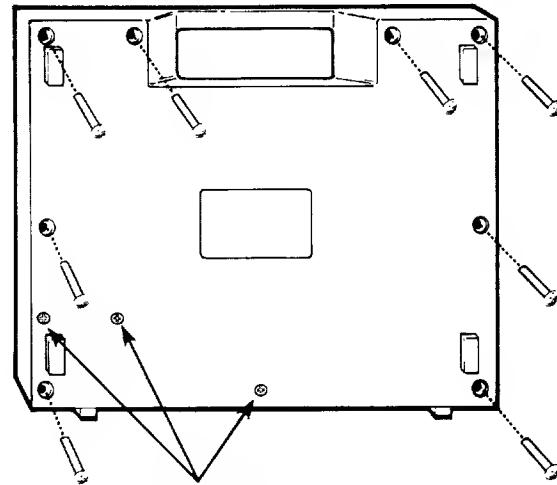
- d. Return the programmer to its normal upright position (as if you were going to operate it.)
- e. Firmly grip and pull up on the top left and right hand sides of the programmer; pulling the top panel towards you.
- f. Lay both disassembled sections of the programmer on a flat surface.

**4-1a)** Turn the programmer so that the rear panel faces you. Remove the screw located in the top-central portion of the panel.



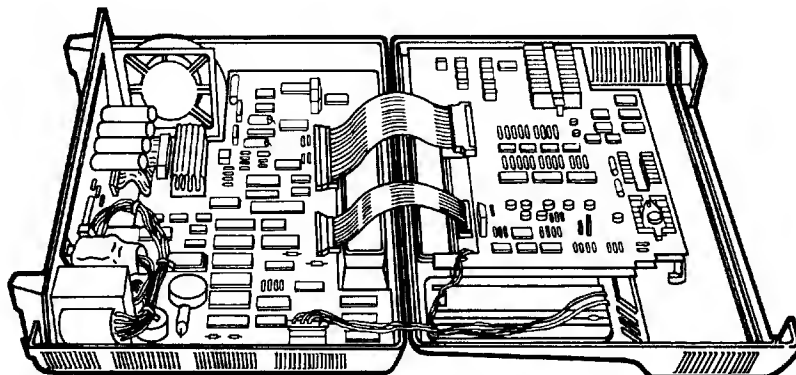
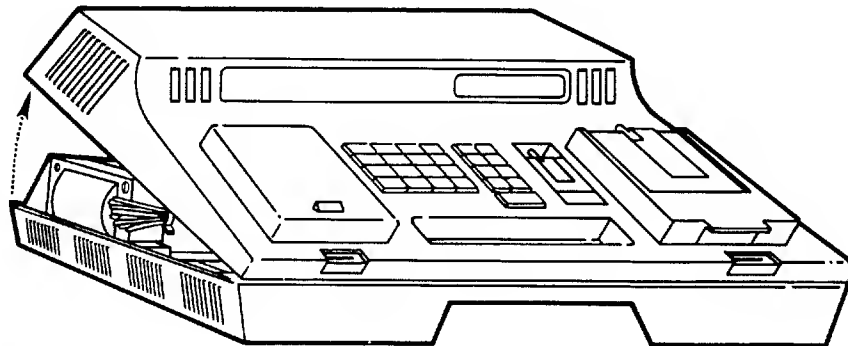
**4-1b)** Stand the programmer on end so that the bottom faces you. Remove the 8 screws from the bottom of the programmer.

**CAUTION**  
During reassembly, do not overtighten these 8 screws (9.0 in-lb max).



**WARNING**  
Do not remove these screws.

**4-1c)** Return the programmer to its normal upright position. To gain access to the test points and adjustment locations inside the 22A; pull the back of the programmer up and towards you.



**4-1d)** Lay both disassembled sections on a flat surface.

**Figure 4-1. Disassembly of the 22A**



### 4.3.1 DC CALIBRATION

The DC calibration procedures described in this section enable you to check and adjust critical DC voltage levels generated by the 22A. To follow these procedures, use the measurement chart at the end of this section. This measurement chart contains the information necessary for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- **Step No.**—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- **Test No.**—identifies individual tests.
- **Test Description**—identifies the functions being tested.
- **Measurement Test Location**—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- **Measurement**—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the 22A until the problem is corrected.
- **Adjustment Location**—tells which potentiometer to adjust if a measurement is out of range.
- **Comments**—gives special instructions for particular tests.

The DC calibration procedures are as follows:

1. Remove any devices that may be in either the fixed 28-pin front panel socket, or the socket adapter.
2. If you have not already done so, turn the programmer power on (section 3.2).
3. Put the programmer in the calibration mode. The key sequence for doing this is:
  - a. Press SELECT.
  - b. Enter C1
  - c. Press START to execute calibration step 1 (or to increment step number).
  - d. To jump ahead to an advanced calibration step, enter the desired calibration step number and press START.
  - e. Decrement a calibration step by pressing REVIEW.
4. Perform the calibration steps on the measurement chart. For steps 6 through 10, refer to the figures at the end of the measurement chart to observe the bit switch rise waveforms, the DAC step waveforms, and the current DAC step waveform.

For each calibration step on the measurement chart, do the following:

- Take measurement readings at the device sockets or test points indicated in the measurement chart; figure 4-2 shows the pin numbers for the device sockets; figure 4-3 shows test points.
- Ground the digital voltmeter to pin 14 on the fixed 28-pin front panel socket.

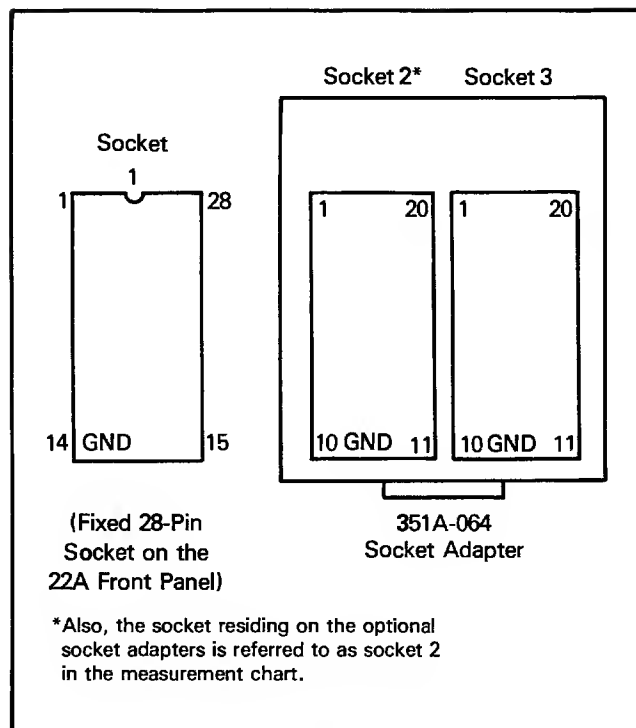


Figure 4-2. Pin Numbers of the Device Sockets

- The adjustment pots on the waveform generator and controller boards enable you to make adjustments when your measurements do not match the measurement chart; figure 4-3 shows the location of these adjustment points.
- Access each new step by pressing the START key. The new step number will appear in the display. To go back to a previous test, press the REVIEW key.

### 4.3.2 OPTIONAL VERIFY-VOLTAGE CHECKS

Two calibration steps (19 and 20) have been provided to enable you to measure first and second pass verify voltages. The family characteristics table in the applicable family timing diagram (at the end of this section) defines the levels for first and second pass verifications for each family. These are provided to help you investigate yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

### 4.3.3 WAVEFORM OBSERVATION

#### NOTE

1. Steps 21-22 are family specific. These steps are optional and have been included for your convenience.
2. When observing waveform E2 (chip select) during address transition, it may momentarily go to VIH. Refer to the appropriate timing diagram.

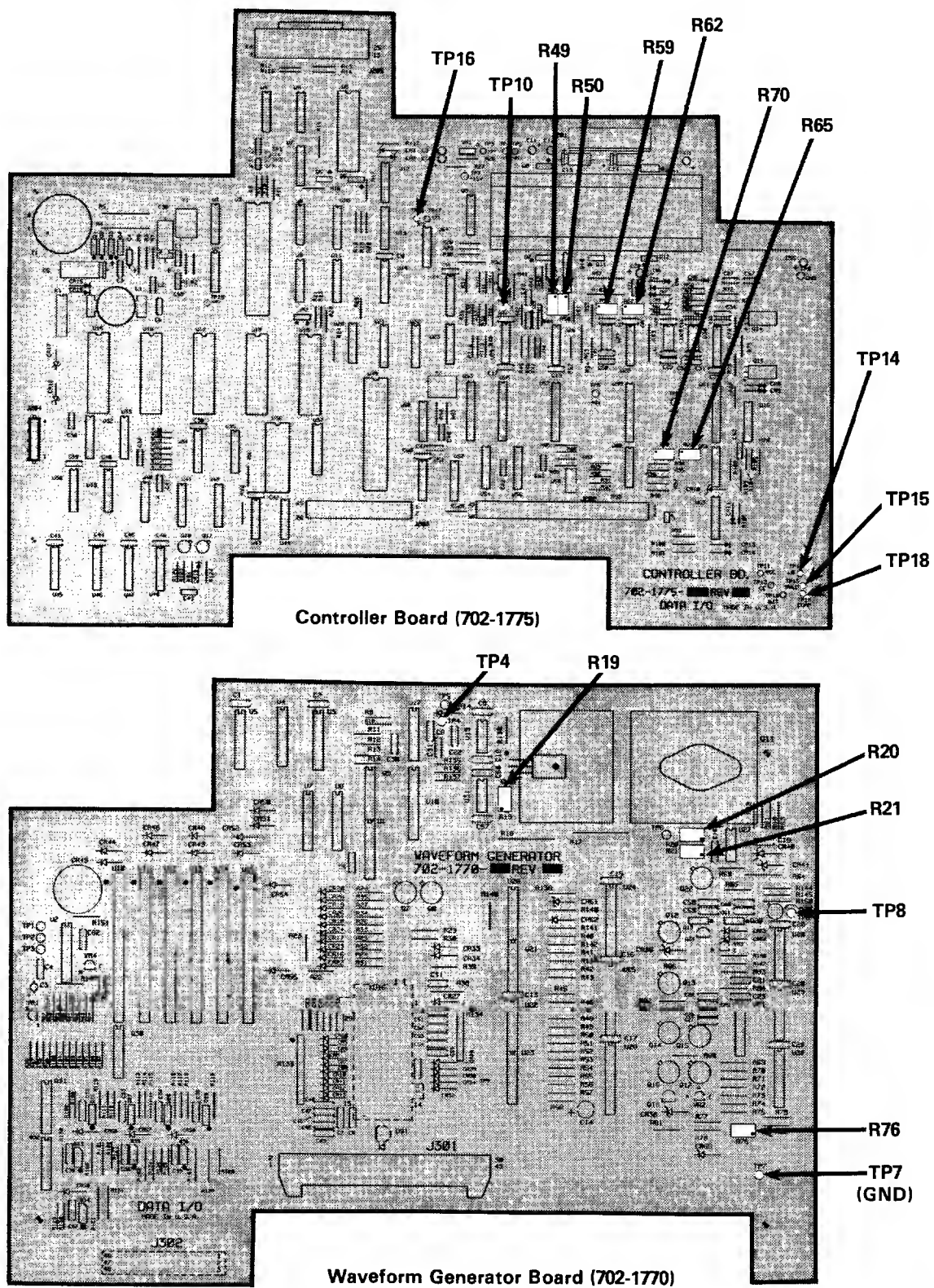


Figure 4-3. Adjustment and Test Point Locations

You can observe the programming waveforms of your 22A with an oscilloscope and can compare them with the timing diagrams that have been provided at the end of this section. In this way, you can measure and compare the timing and magnitude relationships against known specifications to confirm that the 22A is performing to the device manufacturer's specifications. Since the 22A generates a large number of waveforms, and all calibration adjustments are accomplished in DC calibration, it is only necessary to observe waveforms for commonly used devices or those that have yield problems.

During the waveform observation phase of the calibration procedure, your 22A uses a firmware routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated for every address increment. This occurs after the reject pulse count has been reached for all the bits being programmed in the previous data word. The address is automatically reset to 0 when the maximum PROM address is reached, and incrementing continues.

The waveform observation procedure described in this section calls for filling RAM with data so that it is possible to observe bit-to-program waveforms. The procedure takes into account the device type (VOL or VOH) so that for either type of PROM a bit-to-program will appear on the same socket contact.

When used with a timing diagram, this procedure allows you to compare waveforms on the oscilloscope with the waveform photographs on the timing diagram for any type of device; a detailed explanation of the timing diagrams is provided in section 4.3.4. The waveform observation procedure is as follows:

1. Refer to table 1-1 to determine the family and pinout codes.

#### NOTE

*Polarity is indicated in the family code. Odd numbered families are VOL (blank PROM contains logic "1" bits that are selectively programmed to a logic "0" state-output low) and even numbered families are VOH (blank PROM contains logic "0" bits that are selectively programmed to a logic "1" state-output high). If you are in the electronic identifier mode (FF FF), use the last selected algorithm.*

2. Initiate a load operation (copy device to RAM); refer to section 3.4 for details.
3. Key in family and pinout codes when prompted by the programmer.
4. Fill your programmer's RAM (select function A2) with programming data listed in the timing diagram for the family code entered: the correct data depends on the polarity and technology of the device.

#### CAUTION

**Remove all devices before entering the calibration mode at step 5. Waveform generation may damage any device in the socket.**

5. To enter the waveform generation mode at step 21 on the measurement chart:
  - a. Press SELECT
  - b. Enter C1
  - c. Enter 21
  - d. Press START
6. To observe erase waveforms for EEPROMs at step 22 of the measurement chart:
  - a. Press SELECT
  - b. Enter C1
  - c. Enter 22
  - d. Press START
7. Trigger your oscilloscope by connecting to TP16 on 702-1775 board. Refer to figure 4-3.
8. Ground the scope to the ground (GND) contact of the socket with its LED illuminated, the ground contacts are shown in figure 4-2.
9. To observe individual waveforms, refer to figure 4-4 under the pinout code number entered in step 3. The individual socket illustrations give the numbers of the socket contacts to probe when observing the waveforms on the timing diagram.

#### NOTE

*Considerations helpful in setting up and interpreting the waveform displays are explained in section 4.3.4.*

#### 4.3.4 DETAILED EXPLANATION OF THE TIMING DIAGRAMS

This manual contains a timing diagram for each device family that can be programmed by the 22A. Each timing diagram contains a set of waveform photographs that show critical programming parameters. To help you use these diagrams and photographs, read the information that follows and refer to the sample timing diagram (figure 4-4).

1. FAMILY CODE NUMBER—corresponds to the family code number of the device (refer to table 1-1).
2. FAMILY CHARACTERISTIC TABLE—lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered non-critical with a  $\pm 10\%$  tolerance.
3. NOTES—Important information pertaining to a timing diagram.
4. WAVEFORM NAMES—correspond to the pin names on the pinout chart (figure 4-5); the pinout chart tells you which socket pins to probe when you are observing the

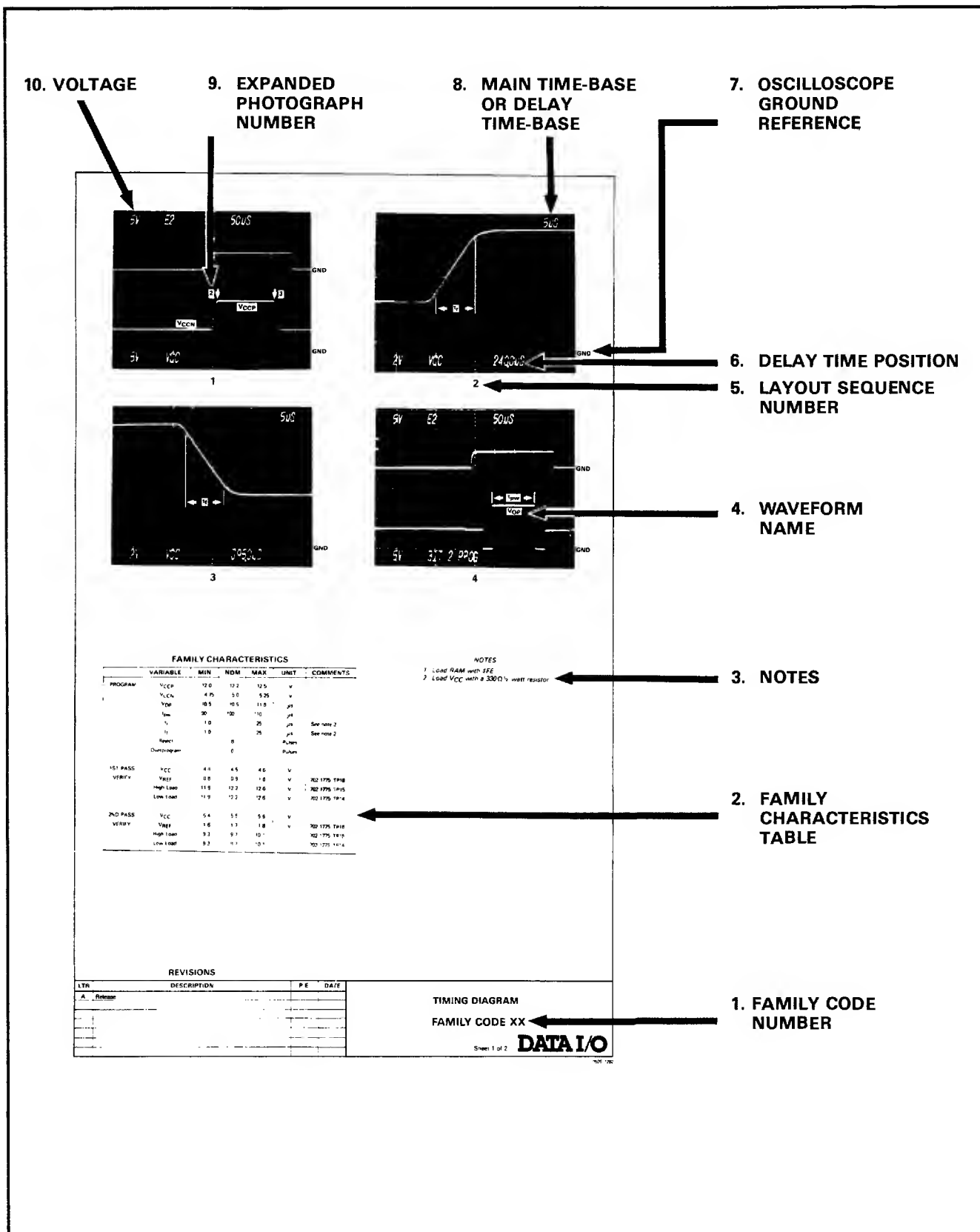


Figure 4-4. Sample Timing Diagram

waveforms for a particular device pinout within a family. (The pinout is indicated by the number above each socket on figure 4-5 which corresponds to the pinout code on table 1-1).

We recommend that you use the oscilloscope's external trigger mode for waveform observation, since one trigger pulse is generated for each address change.

- BIT NO PROG—always use the 02 (bit 2) contact shown on figure 4-5.
  - BIT TO PROG—always use the 01 (bit 1) contact shown on figure 4-5.
5. LAYOUT SEQUENCE NUMBER—used as a reference point within each diagram.
  6. DELAY TIME POSITION—indicates the time from the start of the main sweep to the start of the delay time.
  7. OSCILLOSCOPE GROUND REFERENCE—ground contact on the socket with its LED illuminated.
  8. TIME-BASE AND VOLTS-PER-DIVISION SETTINGS—horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By taking into account any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
  9. EXPANDED PHOTOGRAPH NUMBER—corresponds to the photograph number. These detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train.
  10. VOLTAGE—indicates volts per division. The one in the upper left corner is for the top trace and the one in the lower left corner is for the bottom trace.

## 4.4 TROUBLESHOOTING

The following troubleshooting information is intended to help you interpret and isolate failures in the 22A. It is recommended that you perform a complete calibration before consulting this section. If the problem still persists, use this section along with the information in section 5 (Circuit Description) and the schematics at the end of this manual to isolate and solve the malfunction. Some of the troubleshooting steps that follow require that you gain access to the inside of the programmer. Refer to the disassembly illustrations in figure 4-1.

### 4.4.1 PROGRAMMER DOES NOT POWER UP

If the programmer does not power up:

1. Check that the power supply line fuse is intact (section 2.4.2).
2. Check that the AC power selection is correct (section 2.4.1).

3. Check that all interconnecting cables are plugged into their appropriate receptacles.
4. Check that the fan is operating and that the secondary power supply fuses are good and intact.

### 4.4.2 ERRATIC PROGRAMMER DISPLAY OR NO KEYBOARD RESPONSE

If the programmer display is erratic it usually indicates a problem with the microprocessor, its associated circuitry or one of the memory circuits. Also, if there is no response from keyboard commands, this indicates a problem with the keyboard and/or display circuitry. In this case:

1. Check that all interconnecting cables are plugged into their appropriate receptacles.
2. Verify that all PROMs are installed properly. Also check that there are no bent leads on these socketed PROMs.

### 4.4.3 PROGRAMMER WILL NOT PERFORM A DEVICE-RELATED OPERATION PROPERLY

If the programmer will not perform a device-related operation properly:

1. Check to make sure the correct family and pinout codes are entered. Consult table 1-1.
2. Enter the calibration mode and step through the measurement chart verifying all the voltages in steps 2 through 20.
3. Observe the waveforms according to the instructions in section 4.3.3.

### 4.4.4 PROGRAMMER WILL NOT PERFORM A PORT-RELATED OPERATION PROPERLY

If the programmer will not perform a port-related operation properly:

1. Verify that the correct data translation format code is in effect. Consult table A-2 in Appendix A.
2. Check that the correct baud rate, stop bit(s) and parity setting are in effect. Refer to section 2.6.
3. Check that the RS232 cabling between the programmer and the host/peripheral is in conformance to the instructions in section 2.6.
4. Check the RS232C voltages for the proper levels. Consult table 2-3.
5. Check to make sure the UV lamp is turned off when using the serial paper tape reader.

### 4.4.5 PROGRAMMER ULTRAVIOLET (UV) LAMP WILL NOT ERASE MOS PROMs PROPERLY

#### CAUTION

Always remember to protect your eyes and skin from damaging ultraviolet light rays when following the procedures in this section.

If the UV key on the front panel is depressed, and the UV LED indicator does not light:

1. Check the UV safety interlock switch located on the UV cable assembly (709-0091). The assembly is located under the front panel.

If the UV LED is activated when the UV key is depressed:

1. Check the voltage at pin 4 of the UV lamp driver connector J204. The voltage at this point should be an approximately 35 volts peak at 20 kilohertz. If the voltage is approximately 80 volts peak, then the

problem is either the UV tube itself or the start relay. If the voltage is less than approximately 35 volts, the problem is likely to be associated with the UV drive circuitry.

2. Verify that the start relay is working properly. Do this by measuring, at the moment the UV key is depressed, the voltage at pin 2 of the UV lamp connector J204. The voltage level should be 10 to 20 volts peak for three seconds. The voltage will then drop to 5 volts peak.

<b>01</b> A6 1 16 VCC A5 2 15 A7 A4 3 14 E1 A3 4 13 E2 A0 5 15 O1 A1 6 11 O2 A2 7 10 O3 GND 8 9 O4	<b>02</b> O1 1 16 VCC O2 2 15 E2 O3 3 14 A4 O4 4 13 A3 O5 5 12 A2 O6 6 11 A1 O7 7 10 A0 GND 8 9 O8	<b>03</b> A6 1 16 VCC A5 2 15 A7 A4 3 14 A8 A3 4 13 E2 A0 5 12 O1 A1 6 11 O2 A2 7 10 O3 GND 8 9 O4	<b>05</b> A6 1 18 VCC A5 2 17 A7 A4 3 16 A8 A3 4 15 A9 A0 5 14 O1 A1 6 13 O2 A2 7 12 O3 E1 8 11 O4 GND 9 10 E2	<b>06</b> A6 1 18 VCC A5 2 17 A7 A4 3 16 A8 A3 4 15 A9 A0 5 14 O1 A1 6 13 O2 A2 7 12 O3 A10 8 11 O4 GND 9 10 E2	<b>07</b> A6 1 18 VCC A5 2 17 A7 A4 3 16 A8 A3 4 15 A9 A0 5 14 O1 A1 6 13 O2 A2 7 12 O3 E2 8 11 O4 GND 9 10 CK
<b>08</b> A0 1 20 VCC A1 2 19 A7 A2 3 18 A6 A3 4 17 A5 A4 5 16 E1 A1 6 15 E2 O2 7 14 O8 O3 8 13 O7 O4 9 12 O6 GND 10 11 O5	<b>09</b> A0 1 20 VCC A1 2 19 A8 A2 3 18 A7 A3 4 17 A6 A4 5 16 A5 A1 6 15 E2 O2 7 14 O8 O3 8 13 O7 O4 9 12 O6 GND 10 11 O5	<b>11</b> A6 1 20 VCC A5 2 19 A7 A4 3 18 A8 A3 4 17 A9 A0 5 16 O1 A1 6 15 O2 A2 7 14 O3 A10 8 13 O4 E1 9 12 CK GND 10 11 E2	<b>14</b> A7 1 24 VCC A6 2 23 NC A5 3 22 NC A4 4 21 E1 A3 5 20 E2 A2 6 19 E3 A1 7 18 E4 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>15</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 NC A4 4 21 E1 A3 5 20 E2 A2 6 19 E3 A1 7 18 E4 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>16</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 E1 A3 5 20 E2 A2 6 19 E3 A1 7 18 E4 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4
<b>21</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 A10 A3 5 20 E2 A2 6 19 E3 A1 7 18 E4 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>22</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 VPP A3 5 20 E2 A2 6 19 E1 A1 7 18 PE A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>23</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 VPP A3 5 20 E2 A2 6 19 A10 A1 7 18 PE A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>24</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 A11 A3 5 20 VPP A2 6 19 A10 A1 7 18 PE A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>25</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 VPP A3 5 20 PE A2 6 19 A10 A1 7 18 A11 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>26</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 E1 A4 4 21 VBB A3 5 20 E2 A2 6 19 VOD A1 7 18 VPP A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4
<b>27</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 VBB A3 5 20 E2 A2 6 19 VDD A1 7 18 VPP A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>28</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 VBB A3 5 20 A10 A2 6 19 VDD A1 7 18 VPP A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>29</b> A7 1 24 VCC A6 2 23 A8 A5 3 22 A9 A4 4 21 A12 A3 5 20 VPP A2 6 19 A10 A1 7 18 A11 A0 8 17 O8 O1 9 16 O7 O2 10 15 O6 O3 11 14 O5 GND 12 13 O4	<b>30</b> VPP 1 28 VCC E1 2 27 E2 A7 3 26 NC A6 4 25 A8 A5 5 24 A9 A4 6 23 A12 A3 7 22 PE A2 8 21 A10 A1 9 20 A11 O1 10 19 O8 O2 11 18 O7 O3 12 17 O6 O4 13 16 O5 GND 14 15 O4	<b>31</b> VPP 1 28 VCC A13 2 27 E2 A7 3 26 NC A6 4 25 A8 A5 5 24 A9 A4 6 23 A12 A3 7 22 PE A2 8 21 A10 A1 9 20 A11 A0 10 19 O8 O1 11 18 O7 O2 12 17 O6 O3 13 16 O5 GND 14 15 O4	<b>32</b> VPP 1 28 VCC A12 2 27 A14 A7 3 26 A13 A6 4 25 A8 A5 5 24 A9 A4 6 23 A11 A3 7 22 OE A2 8 21 A10 A1 9 20 CE A0 10 19 O8 O1 11 18 O7 O2 12 17 O6 O3 13 16 O5 GND 14 15 O4

#### CAUTION

To observe a bit-to-program waveform, always use the 01 contact.

To observe a no-bit-to-program waveform, always use 02.

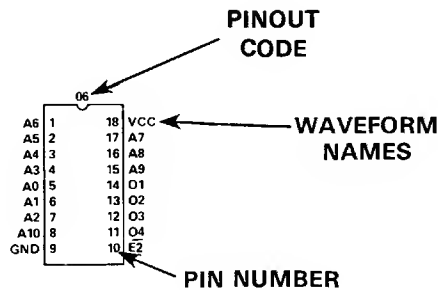


Figure 4-5. Pin Names by Pinout Code

33				35				36				37				38				42			
VPP	1	28	VCC	A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC	A6	1	18	VCC	A7	1	24	VCC
A12	2	27	PGM	A6	2	23	A8	A6	2	23	A8	A6	2	23	A8	A5	2	17	A7	A6	2	23	A8
A7	3	26	NC	A5	3	22	A9	A5	3	22	NC	A5	3	22	A9	A4	3	16	A8	A5	3	22	A9
A6	4	25	A8	A4	4	21	VPP	A4	4	21	E2	A4	4	21	E2	A3	4	15	A9	A4	4	21	NC
A5	5	24	A9	A3	5	20	E2	A3	5	20	E1	A3	5	20	E1	A0	5	14	O1	A3	5	20	E2
A4	6	23	A11	A2	6	19	E3	A2	6	19	E3	A2	6	19	E3	A1	6	13	O2	A2	6	19	A10
A3	7	22	DE	A1	7	18	PE	A1	7	18	E4	A1	7	18	E4	A2	7	12	O3	A1	7	18	E1
A2	8	21	A10	A0	8	17	O8	A0	8	17	O8	A0	8	17	O8	E2	8	11	O4	A0	8	17	O8
A1	9	20	CE	O1	9	16	O7	O1	9	16	O7	O1	9	16	O7	GND	9	10	ET	O1	9	16	O7
A0	10	19	O8	O2	10	15	O6	O2	10	15	O6	O2	10	15	O6					O2	10	15	O6
O1	11	18	O7	O3	11	14	O5	O3	11	14	O5	O3	11	14	O5					O3	11	14	O5
O2	12	17	O6	GND	12	13	O4	GND	12	13	O4	GND	12	13	O4					GND	12	13	O4
O3	13	16	O5																				
CND	14	15	O4																				

43				46				47				49				50				51			
A7	1	24	VCC	A0	1	20	VCC	A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC	VPP	1	28	VCC
A6	2	23	E5	A1	2	19	A7	A6	2	23	A8	A6	2	23	A8	A6	2	23	A8	A12	2	27	PGM
A5	3	22	NC	A2	3	18	A6	A5	3	22	E1	A5	3	22	A9	A5	3	22	A9	A7	3	26	A13
A4	4	21	ET	A3	4	17	A5	A4	4	21	E2	A4	4	21	A11	A4	4	21	VPP	A6	4	25	A8
A3	5	20	E2	A4	5	16	E2	A3	5	20	E3	A3	5	20	VPP	A3	5	20	CK	A5	5	24	A9
A2	6	19	E3	O1	6	15	E1	A2	6	19	CK	A2	6	19	A10	A2	6	19	A10	A4	6	23	A11
A1	7	18	E4	O2	7	14	O8	A1	7	18	VPP	A1	7	18	CK	A1	7	18	A11	A3	7	22	OE
A0	8	17	O8	O3	8	13	O7	A0	8	17	O8	A0	8	17	O8	A0	8	17	O8	A2	8	21	A10
O1	9	16	O7	O4	9	12	O6	O1	9	16	O7	O1	9	16	O7	O1	9	16	O7	A1	9	20	CE
O2	10	15	O6	CND	10	11	O5	O2	10	15	O6	O2	10	15	O6	O2	10	15	O6	A0	10	19	O8
O3	11	14	O5					O3	11	14	O5	O3	11	14	O5	O3	11	14	O5	O1	11	18	O7
CND	12	13	O4					CND	12	13	O4	GND	12	13	O4	CND	12	13	O4	O2	12	17	O6

53				55				56, 59				57				58			
A8	1	20	VCC	PGM	1	40	VCC	E2	1	40	VCC	E2	1	40	VCC	A0	1	40	VCC
A7	2	19	A9	E3	2	39	NC	XTAL 1	2	39	NC	XTAL 1	2	39	NC	A1	2	39	O1
A6	3	18	A10	E1	3	38	NC	XTAL 2	3	38	NC	XTAL 2	3	38	NC	A2	3	38	O2
A5	4	17	A11	E4	4	37	NC	CLK	4	37	NC	CLK	4	37	NC	A3	4	37	O3
A4	5	16	ET	VDD	5	36	NC	E4	5	36	NC	E4	5	36	NC	A4	5	36	O4
A3	6	15	E2	E5	6	35	NC	E3	6	35	NC	E3	6	35	NC	A5	6	35	O5
A2	7	14	O1	E8	7	34	NC	EA	7	34	NC	EA	7	34	NC	A6	7	34	O6
A1	8	13	O2	E7	8	33	NC	E5	8	33	NC	E5	8	33	NC	A7	8	33	O7
A0	9	12	O3	E2	9	32	NC	E1	9	32	NC	E1	9	32	NC	ET	9	32	O8
CND	10	11	O4	E8	10	31	NC	E6	10	31	NC	E8	10	31	NC	NC	10	31	VPP
				CLK	11	30	NC	E7	11	30	NC	E7	11	30	NC	NC	11	30	PGM
				O1	12	29	NC	O1	12	29	NC	O1	12	29	NC	NC	12	29	GND
				O2	13	28	NC	O2	13	28	GND	O2	13	28	GND	NC	13	28	E2
				O3	14	27	NC	O3	14	27	GND	O3	14	27	GND	NC	14	27	GND
				O4	15	26	NC	O4	15	26	VDD	O4	15	26	VDD	NC	15	26	GND
				O5	16	25	NC	O5	16	25	VPP	O5	16	25	VPP	NC	16	25	GND
				O6	17	24	NC	O6	17	24	NC	O6	17	24	NC	NC	17	24	A11
				O7	18	23	A10	O7	18	23	NC	O7	18	23	A10	XTAL 2	18	23	A10
				O8	19	22	A9	O8	19	22	A9	O8	19	22	A9	XTAL 1	19	22	A8
				CND	20	21	A8	GND	20	21	A8	GND	20	21	A8	GND	20	21	A8

60				61				62				63				64				65			
A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC	A7	1	24	VCC
A6	2	23	A8	A6	2	23	A8	A6	2	23	A8	A6	2	23	A8	A6	2	23	A8	A6	2	23	A8
A5	3	22	A9	A5	3	22	VIL	A5	3	22	E4	A5	3	22	A9	A5	3	22	A9	A5	3	22	E3
A4	4	21	E3	A4	4	21	E1	A4	4	21	E3	A4	4	21	A10	A4	4	21	ET	A4	4	21	E2
A3	5	20	ET	A3	5	20	E2	A3	5	20	ET	A3	5	20	E2	A3	5	20	E2	A3	5	20	E4
A2	6	19	NC	A2	6	19	NC	A2	6	19	NC	A2	6	19	A11	A2	6	19	A10	A2	6	19	ET
A1	7	18	E2	A1	7	18	E2	A1	7	18	F2	A1	7	18	E3	A1	7	18	VPP	A1	7	18	CP
A0	8	17	O8	A0	8	17	O8	A0	8	17	O8	A0	8	17	O8	A0	8	17	O8	A0	8	17	O8
O1	9	16	O7	O1	9	16	O7	O1	9	16	O7	O1	9	16	O7	O1	9	16	O7	O1	9	16	O7
O2	10	15	O6	O2	10	15	O6	O2	10	15	O6	O2	10	15	O6	O2	10	15	O6	O2	10	15	O6
O3	11	14	O5	O3	11	14	O5	O3	11	14	O5	O3	11	14	O5	O3	11	14	O5	O3	11	14	O5
CND	12	13	O4	GND	12	13	O4	GND	12	13	O4	CND	12	13	O4	GND	12	13	O4	CND	12	13	O4

Figure 4-5. Pin Names by Pinout Code (Continued)



66			
A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	E2
A3	5	20	E3
A2	6	19	E1
A1	7	18	CK
AO	8	17	O8
O1	9	16	O7
O2	10	15	O6
O3	11	14	O5
GND	12	13	O4

67			
A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	A10
A3	5	20	E2
A2	6	19	A11
A1	7	18	A12
AO	8	17	O8
O1	9	16	O7
O2	10	15	O6
O3	11	14	O5
GND	12	13	O4

68			
A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	A10
A3	5	20	E2
A2	6	19	E3
A1	7	18	E4
AO	8	17	O8
O1	9	16	O7
O2	10	15	O6
O3	11	14	O5
GND	12	13	O4

69			
A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	NC
A3	5	20	E2
A2	6	19	NC
A1	7	18	E1
AO	8	17	O8
O1	9	16	O7
O2	10	15	O6
O3	11	14	O5
GND	12	13	O4

70			
VPP	1	28	VCC
N C	2	27	E3
A7	3	26	N C
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	E1
A2	8	21	A10
A1	9	20	PE
AO	10	19	O8
O1	11	18	O7
O2	12	17	O6
O3	13	16	O5
GND	14	15	O4

71			
VPP	1	28	VCC
N C	2	27	E3
A7	3	26	N C
A6	4	25	A8
A5	5	24	A9
A4	6	23	N C
A3	7	22	E1
A2	8	21	A10
A1	9	20	PE
AO	10	19	O8
O1	11	18	O7
O2	12	17	O6
O3	13	16	O5
GND	14	15	O4

72			
VPP	1	28	VCC
N C	2	27	E3
A7	3	26	N C
A6	4	25	A8
A5	5	24	A9
A4	6	23	N/C
A3	7	22	E1
A2	8	21	N/C
A1	9	20	PE
AO	10	19	O8
O1	11	18	O7
O2	12	17	O6
O3	13	16	O5
GND	14	15	O4

75			
A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	PGM
A3	5	20	VPP
A2	6	19	A10
A1	7	18	CLK
AO	8	17	O8
O1	9	16	O7
O2	10	15	O6
O3	11	14	O5
GND	12	13	O4

76			
A8	1	20	VCC
A7	2	19	A9
A6	3	18	A10
A5	4	17	A11
A4	5	16	CLK
A3	6	15	CLK
A2	7	14	O1
A1	8	13	O2
AO	9	12	O3
GND	10	11	O4

88			
E2	1	40	VCC
XTAL 1	2	39	NC
XTAL 2	3	38	NC
CLK	4	37	NC
E4	5	36	NC
E3	6	35	NC
EA	7	34	NC
E5	8	33	NC
E1	9	32	NC
E6	10	31	NC
E7	11	30	NC
O1	12	29	NC
O2	13	28	GND
O3	14	27	GND
O4	15	26	VDD
O5	16	25	VPP
O6	17	24	A11
O7	18	23	A10
O8	19	22	A9
GND	20	21	A8

Figure 4-5. Pin Names by Pinout Code (Continued)

## MEASUREMENT CHART

# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RDP	5/15/82

## 22 Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Circuit Boards/ Socket/Pins Test Points	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS
				MIN	NOM	MAX		
1	1	All voltages off	All	-0.1V		0.4V	R70 702-1775	Factory only. Adjust pot fully counter-clockwise.
2	2	V reference	702-1775/TP10	4.80V		5.20V		
	3	Comparator reference	702-1775/TP18	1.45V	1.50V	1.55V	R49 702-1775	Adjust in order of occurrence.
	4	Load supply	702-1775/TP14	17.5V	18.0V	18.5V	R50 702-1775	
	5	CE supply	1/20	32.9V	33.0V	33.1V	R62 702-1775	No load condition.
	6	V <sub>CC</sub> supply	1/28	4.95V	5.00V	5.05V	R65 702-1775	No load condition.
	7	Bit supply	1/11	25.9V	26.0V	26.1V	R59 702-1775	No load condition.
	8	Clamp supply	702-1770/TP4	25.3V	25.4V	25.5V	R19 702-1770	Turn pot counter-clockwise until voltage is .2V greater than nominal value; then turn clockwise until voltage just reaches nominal value.
	9	Socket 1 LED						Confirm socket 1 LED on.
	10	V <sub>CC</sub> supply loaded(250ma)	1/28	4.90V		5.05V		Place a 20 ohm, 2 watt resistor between pin 14 and 28, socket 1.
	11	CE supply loaded	1/20	32.5V		33.1V		Place 135 ohm, 10 watt resistor between pin 14 and 20, socket 1.
	12	Bit supply loaded	1/11	25.3V		26.1V		Place 110 ohm, 10 watt resistor between pin 14 and 11, socket 1.

Note: 1. For steps 1 - 18 ground reference is pin 14 on the fixed 28-pin front panel socket. For steps 19 - 22, the ground reference is the pin in the bottom left-hand corner of the socket with its LED illuminated.  
2. All load resistors should be  $\pm 1\%$  of nominal value.

3. Reference to Socket 1 in this chart means the programmer's fixed 28-pin front panel socket. Socket 2 is the left socket on socket adapter 351A-064 or the socket on optional socket adapters. Socket 3 refers to the right socket on socket adapter 351A-064.

# REVISIONS

LTR	DESCRIPTION	P.E.	DATE					
	See Sheet 1			22 Measurement Chart				
STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Circuit Boards/ Socket/Pins Test Points	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS
				MIN	NOM	MAX		
3	13	V <sub>CC</sub> supply current(50ma)	1/28	4.93V		5.05V	R70 702-1775	Place 100 ohm, 1/4 watt resistor between pin 14 and 28; adjust pot clockwise just until error 31 displayed.
	14	Clamp supply	702-1770/TP4	25.3V		25.5V		
	15	Load supply	702-1775/TP14	3.75V		4.25V		
	16	SW load supply off	702-1775/TP15	-0.1V		0.4V		
	17	20ma current source	1/11	19.5ma	20.0ma	20.5ma	R21 702-1770	Place current meter in series with a 100 ohm, 2 watt resistor, pin 11 to 14.
4	18	Program current source	1/11	118ma	120ma	122ma	R20 702-1770	Ground TP8 on 702-1770, load same as 20ma test.
	19	Load supply	702-1775/TP14	3.75V		4.25V		
	20	SW load supply off	702-1775/TP15	-0.1V		0.4V		
5	21	SW load supply on	702-1775/TP15	8.50V		9.25V		
	22	Comparator reference	702-1775/TP18	7.45V	7.50V	7.55V	R49 702-1775	Readjust reference DAC. Override Step 2 adjustment.
6	23	Bit switch rise rate 3	1/11	62us	65us	68us	R76 702-1770	Adjust pot for rise time between 3V and 30V on rising edge of second slowest rise rate.

# REVISIONS

LTR	DESCRIPTION	P.E.	DATE					
	See Sheet 1							
STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pins      Circuit Boards/ Test Points	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS
				MIN	NOM	MAX		
	24	Bit switch rise rate 1	1/11	1us		3us		Fastest - See waveform photo #11.
	25	Bit switch rise rate 2	1/11	20us		36us		Second fastest-See photo #11.
	26	Bit switch rise rate 4	1/11	70us		120us		Slowest-See photo #11.
7	27	CE switch rise rate 1	1/20	1us		3us		Fastest-See waveform photo #10.
	28	CE switch rise rate 2	1/20	50us		80us		Slowest-See waveform photo #10.
8	29	V <sub>CC</sub> supply DAC step	1/28					See waveform photo #1.
	30	Bit supply DAC step	1/11					See waveform photo #7.
	31	CE supply DAC step	1/20					See waveform photo #4.
	32	Load supply DAC step						See waveform photo #5.
	33	Comparator ref DAC step						See waveform photo #9.
9	34	V <sub>CC</sub> current DAC step	U31 pin 8      702-1775					See waveform photo #2.
	35	Program current DAC step	1/11					Ground TP8 on 702-1770. See
								photo #6.
	36	Clamp supply DAC step						See photo #3.
10	37	Program current pulse	1/11	7.4us		7.6us		Place a 100 ohm, 2 watt resistor
								between pin 11 and pin 14.
								See waveform photo #8.
11	38	Socket 2 LED*						Confirm socket 2 LED on.

22 Measurement Chart

\* Applicable to all socket adapters.

## REVISIONS

[illegible]

\*\* Applicable only to dual 20-pin socket adapter 351A-064.

# REVISIONS

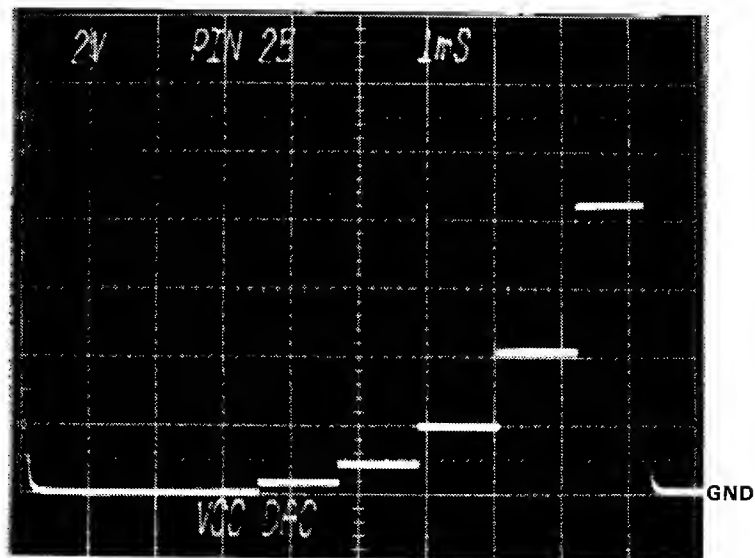
LTR	DESCRIPTION		P.E.	DATE	22 Measurement Chart				
	See Sheet 1								
STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pins Circuit Boards/ Test Points	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS	
				MIN	NOM	MAX			
15	51	Odd pins low	1/1,3,5,7,9,11,13,15,17,19,21,23,25,27,14	-0.1V		0.4V			
	52	Even pins TTL high	1/2,4,6,8,10,12,16,18,20,22,24,26,28	3.0V		5.5V			
16	53	Odd pins to prog V	1/1,9,11,13,15,17,19,21,23	19V		21V		Measure 5V at TP14 on 702-1775,	
	54	Even pins TTL high	1/2-8,10,12,16,18,20,22,24-28	3.0V		5.5V		and 0V at TP15 on 702-1775.	
17	55	Odd pins TTL high	1/1-8,9,11,13,15,17,19,21,23,25-28	3.0V		5.5V		Measure 5V at TP14 on 702-1775,	
	56	Even pins to prog V	1/10,12,16,18,20,22,24	19V		21V		and 0V at TP15 on 702-1775.	
18	57	Pull up/Pull down	1/9-13,15-19,21,24	1.5V		2.5V			
19	58	Static 1st pass						See applicable timing diagram	
		verify levels						photos.	
20	59	Static 2nd pass						See applicable timing diagram	
		verify levels						photos.	
21	60	Program waveforms						See applicable timing diagram	
								photos.***	
22	61	Erase waveforms						See applicable timing diagram	
								photos.***	

\*\*\* Scope trigger point is TP16 on 702-1775 Board for steps 21 and 22.

# Measurement Chart

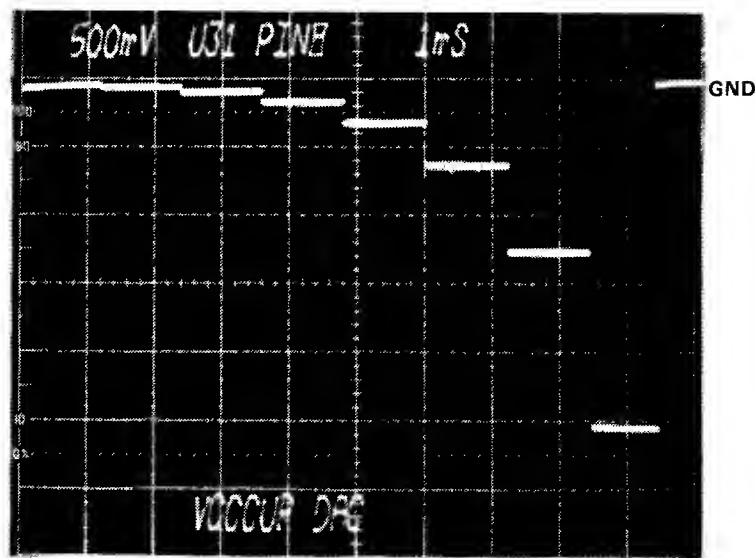
PROGRAM ELECTRONICS

MODEL 22



VCC Supply DAC Step Waveform

1

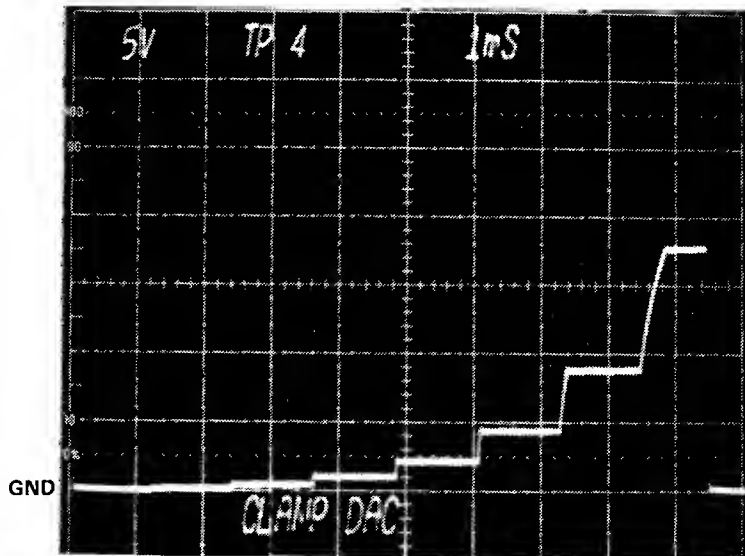


VCC Current Supply DAC Step Waveform

2

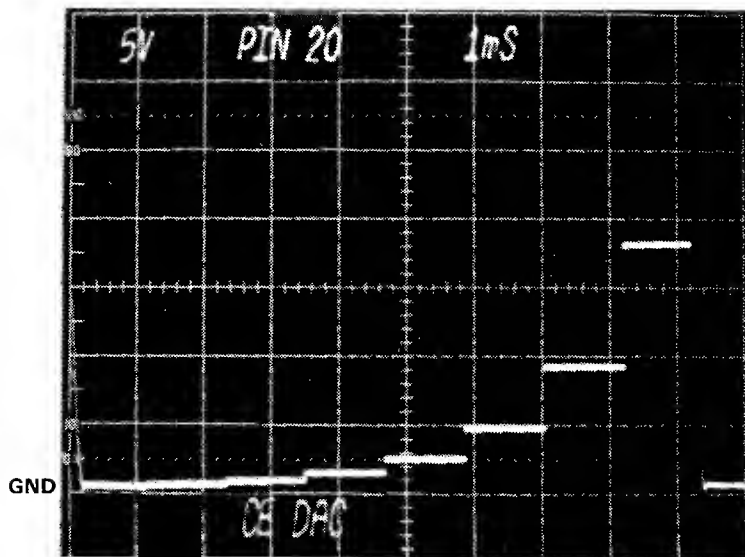


DATE	REV	REVISION RECORD	DR	CK
5/83	A			<i>RL</i>



Clamp Supply DAC Step Waveform

3

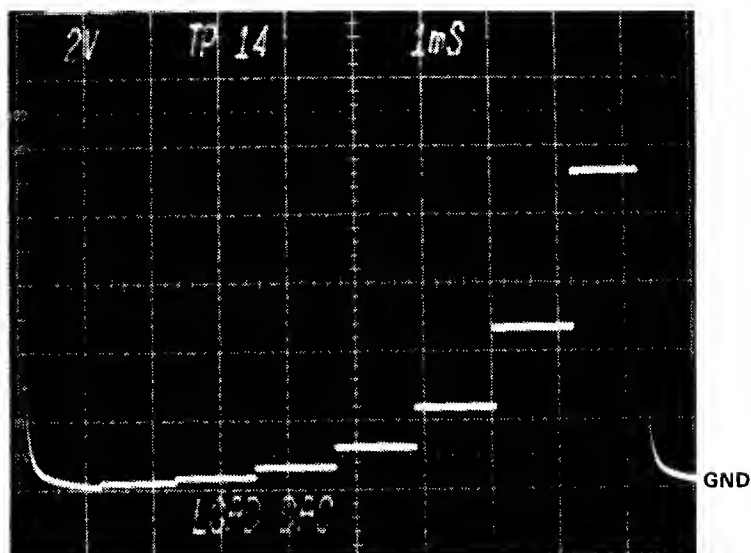


Chip Enable Supply DAC Step Waveform

4

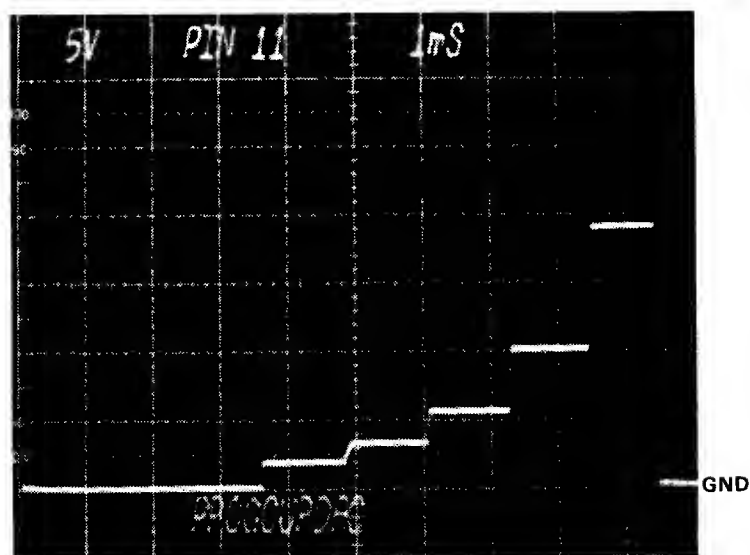
# Measurement Chart

PROGRAM ELECTRONICS MODEL 22



Load Supply DAC Step Waveform

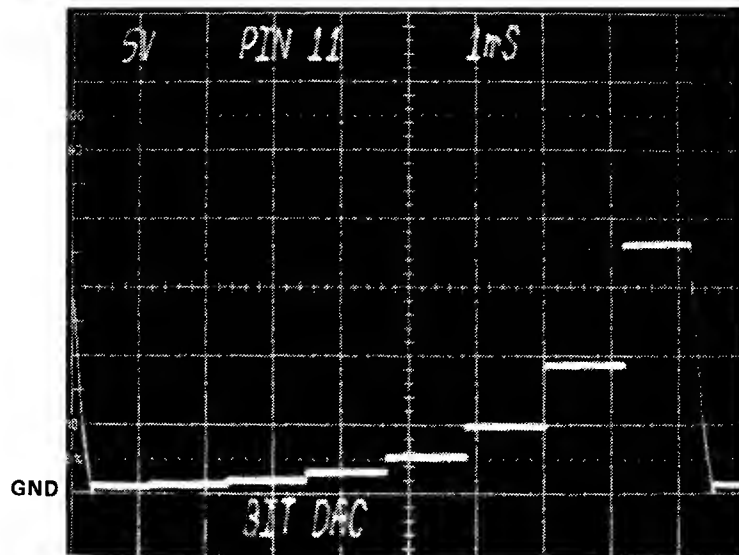
5



Program Current Supply DAC Step Waveform

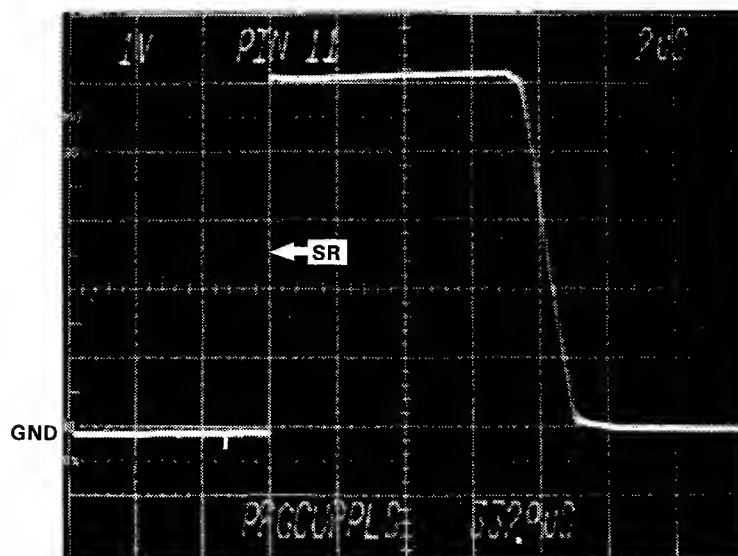
6

DATE	REV	REVISION RECORD	DR	CK
5/83	A			RL



Bit Supply DAC Step Waveform

7

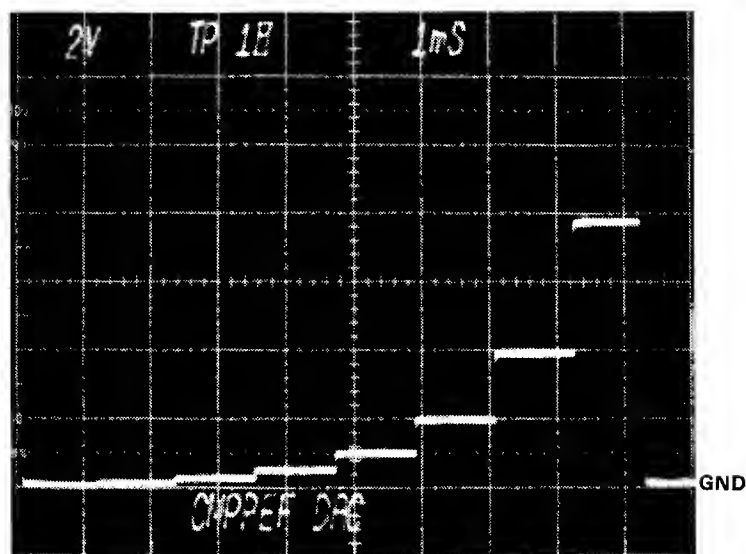


Program Current Pulse

8

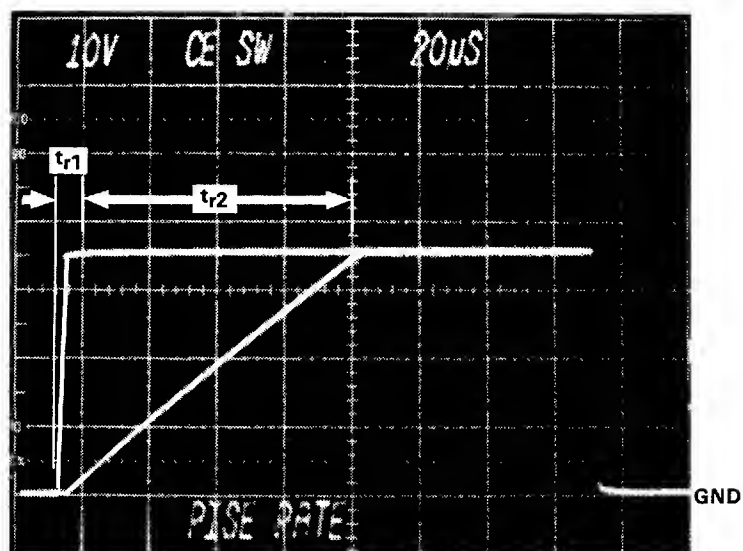
# Measurement Chart

PROGRAM ELECTRONICS MODEL 22



Comparator Reference DAC Step Waveform

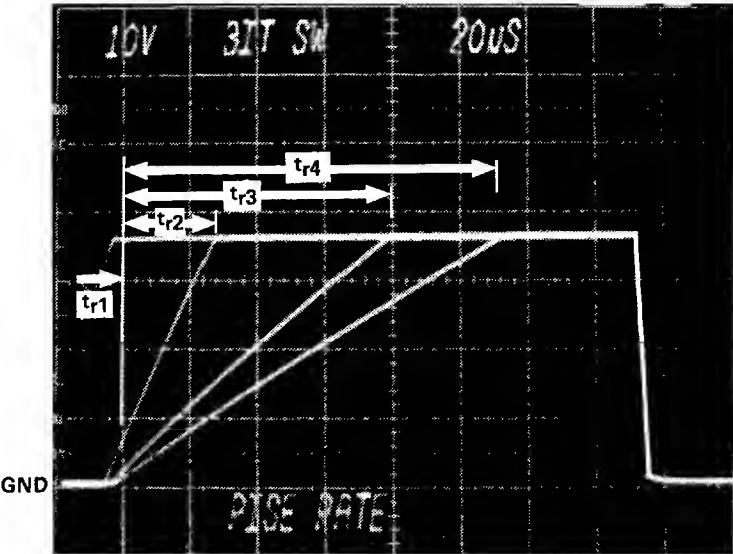
9



Chip Enable Switch Rise Rates

10

	DATE	REV	REVISION RECORD	DR	CK
	5/83	A			RA

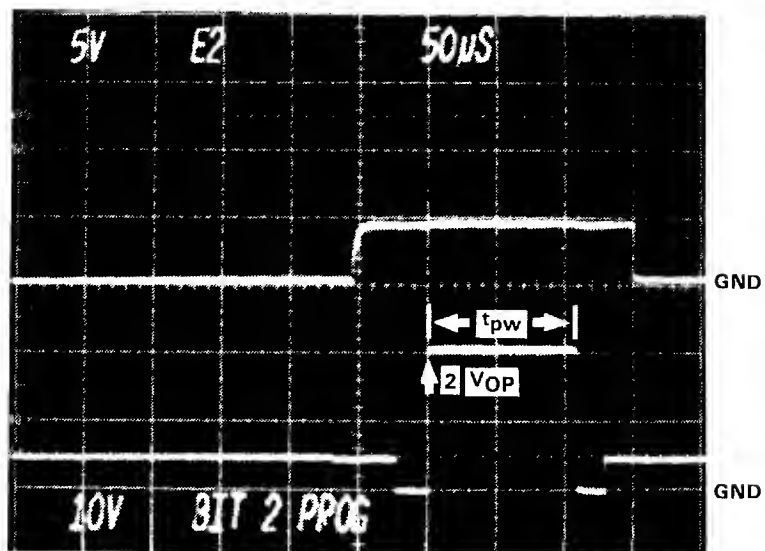


Bit Switch Rise Rates

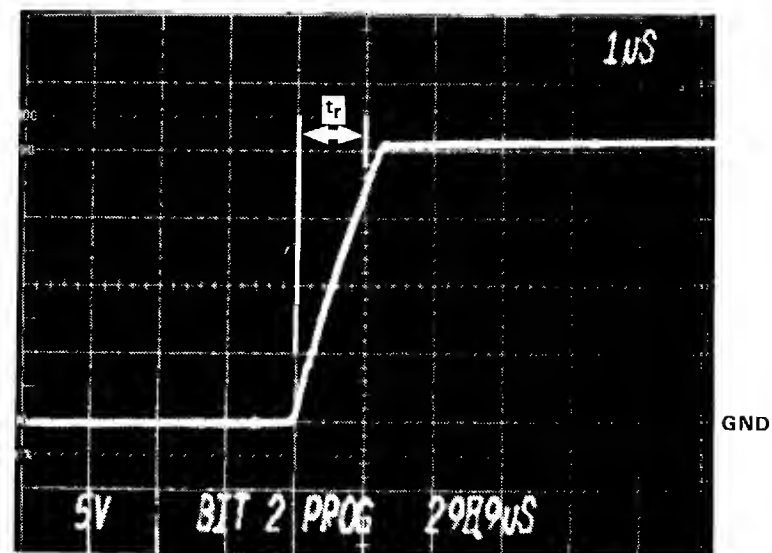
11

Bit Switch Rise Rates					
VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
t <sub>r1</sub>	1		3	μs	P. 11, Sock. 1
t <sub>r2</sub>	20		36	μs	
t <sub>r3</sub>	62	65	68	μs	
t <sub>r4</sub>	70		120	μs	
CE Switch Rise Rates					
t <sub>r1</sub>	1		3	μs	P. 20, Sock. 1
t <sub>r2</sub>	50		80	μs	
Program Current Pulse					
S <sub>R</sub>	50		70	V/μs	100Ω Load P.11,Sock.1

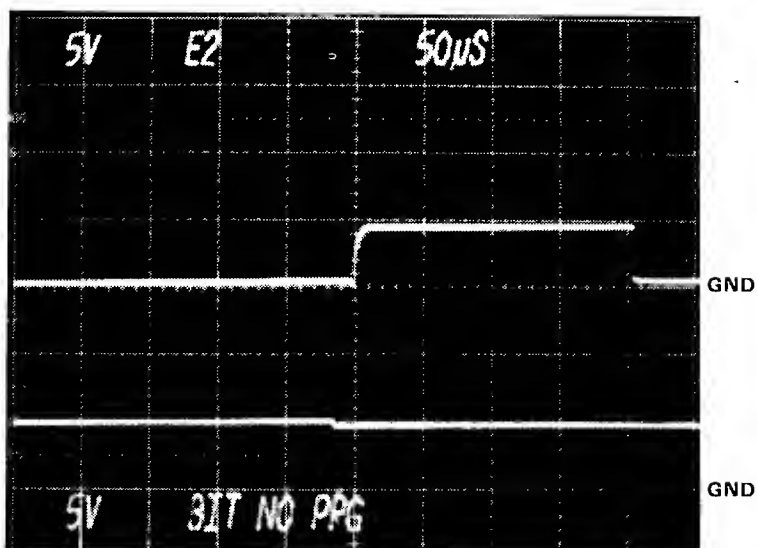
## TIMING DIAGRAMS



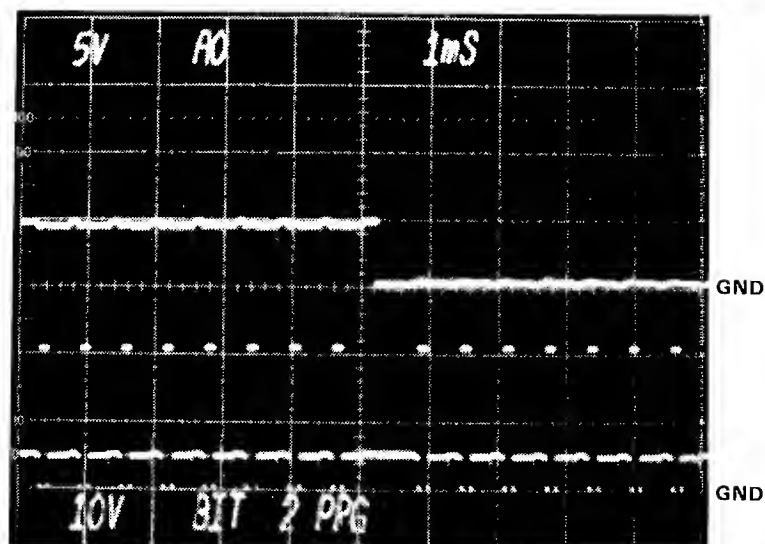
1



2



3



4

# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not Shown
	V <sub>OP</sub>	20.0	20.5	21.0	V	
	t <sub>pw</sub>	90	100	110	μs	
	t <sub>r</sub>	0.5	1.0	3.0	μs	
	t <sub>f</sub>					
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.3	4.4	4.5	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	0.8	0.9	1.0	V	
	High Load	5.4	5.8	6.2	V	
	Low Load	5.4	5.8	6.2	V	
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	0.8	0.9	1.0	V	
	High Load	5.4	5.8	6.2	V	
	Low Load	5.4	5.8	8.2	V	

## NOTES

1. Load RAM with \$FE.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RJA	5/25/83

TIMING DIAGRAM

FAMILY CODE 01

Sheet 1 of 1

**DATA I/O**





# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	12.0	12.2	12.5	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	10.5	10.5	11.0	μs	
	t <sub>pw</sub>	90	100	110	μs	
	t <sub>r</sub>	1.0		25	μs	See note 2
	t <sub>f</sub>	1.0		25	μs	See note 2
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.4	4.5	4.6	V	
VERIFY	V <sub>REF</sub>	0.8	0.9	1.0	V	702-1775/TP18
	High Load	11.9	12.2	12.6	V	702-1775/TP15
	Low Load	11.9	12.2	12.6	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.4	5.5	5.6	V	
VERIFY	V <sub>REF</sub>	1.6	1.7	1.8	V	702-1775/TP18
	High Load	9.3	9.7	10.1		702-1775/TP15
	Low Load	9.3	9.7	10.1		702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. Load V<sub>CC</sub> with a 330Ω ½ watt resistor.

## REVISIONS

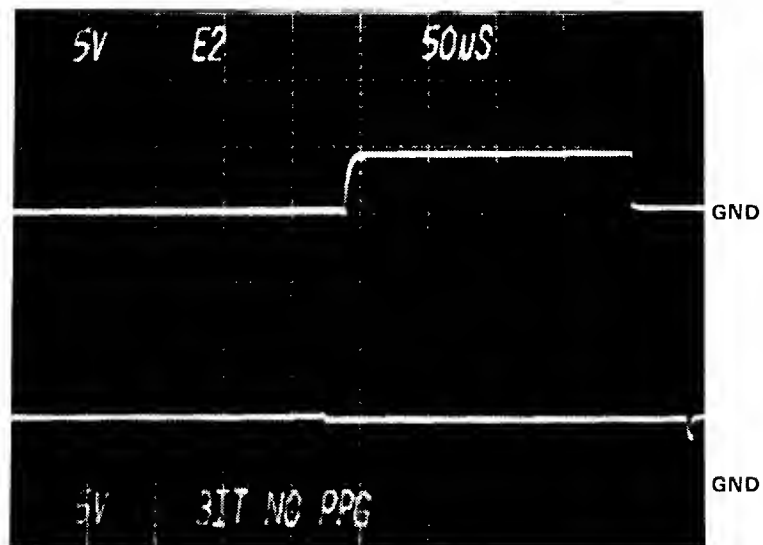
LTR	DESCRIPTION	P.E.	DATE
A	Release	R28	5/25/83

TIMING DIAGRAM

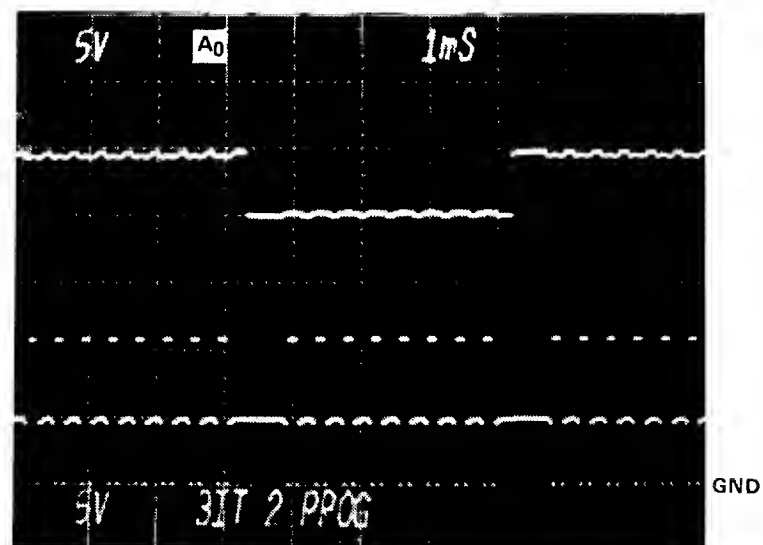
FAMILY CODE 05

Sheet 1 of 2

**DATA I/O**



5



6

REVISIONS

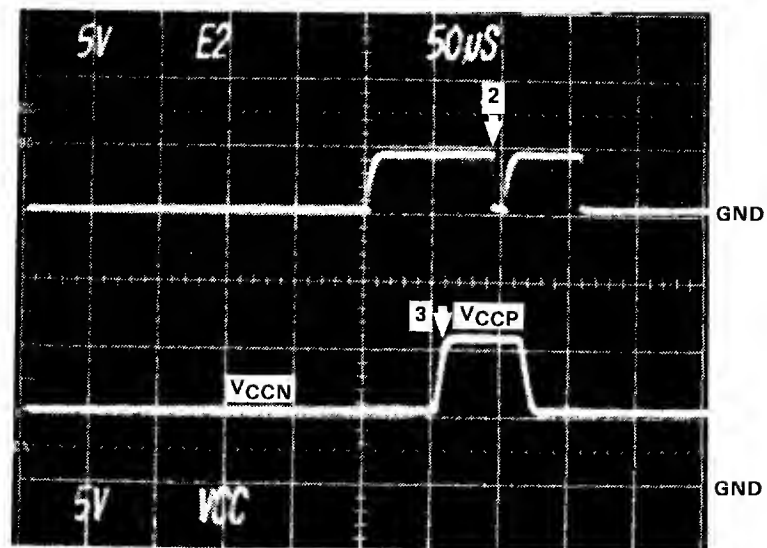
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

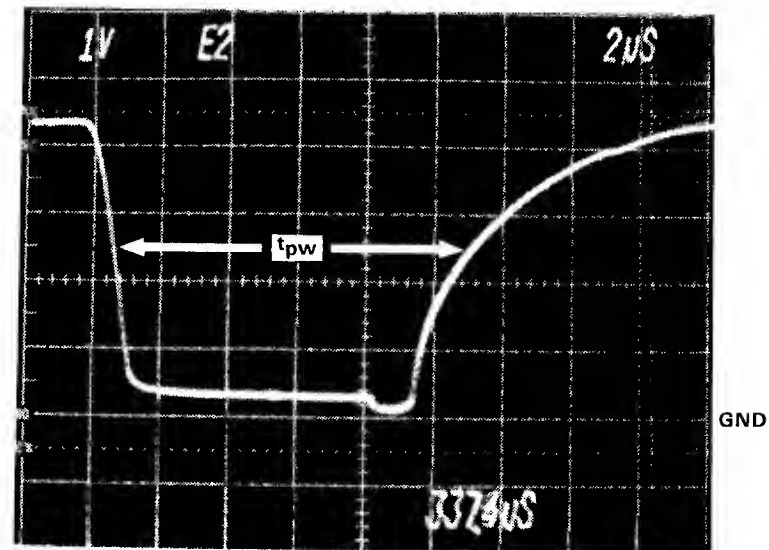
FAMILY CODE 05

Sheet 2 of 2

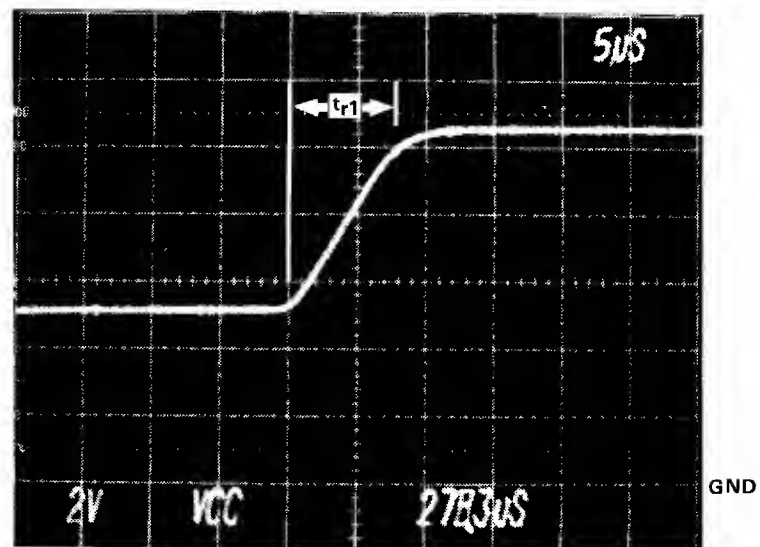
**DATA I/O**



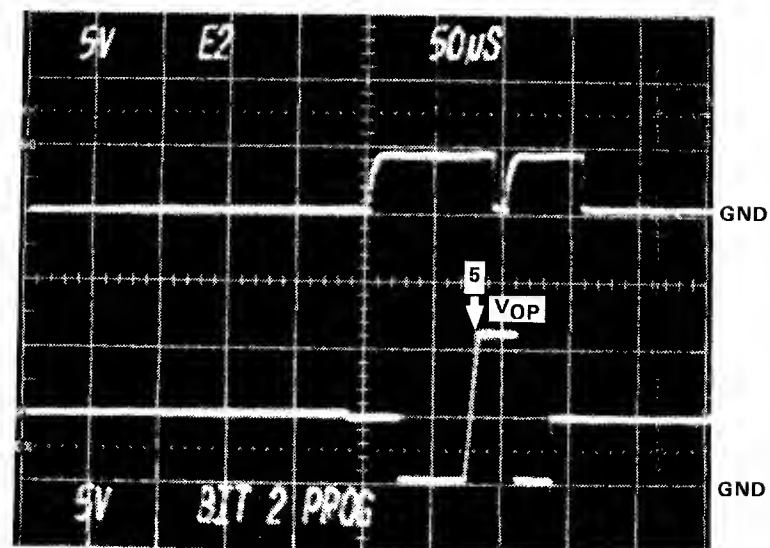
1



2



3



4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	10.0	10.5	11.0	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	10.0	10.5	11.0	μs	
	t <sub>pw</sub>	9.0	10.0	11.0	μs	
	t <sub>r1</sub>	1.0		25	μs	See note 2
	t <sub>r2</sub>	1.0		15	μs	
	t <sub>f</sub>					NA
	Reject		14		Pulses	
	Overprogram		5		Pulses	
1ST PASS	V <sub>CC</sub>	3.9	4.0	4.1	V	
VERIFY	V <sub>REF</sub>	0.8	0.9	1.0	V	702-1775/TP18
	High Load	5.2	5.6	5.9	V	702-1775/TP15
	Low Load	5.2	5.6	5.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.6	1.7	1.8	V	702-1775/TP18
	High Load	4.5	4.9	5.3		702-1775/TP15
	Low Load	4.5	4.9	5.3		702-1775/TP14

## NOTES

1. Load RAM with \$01.
2. Load V<sub>CC</sub> with a 330 Ω ½ watt resistor.

## REVISIONS

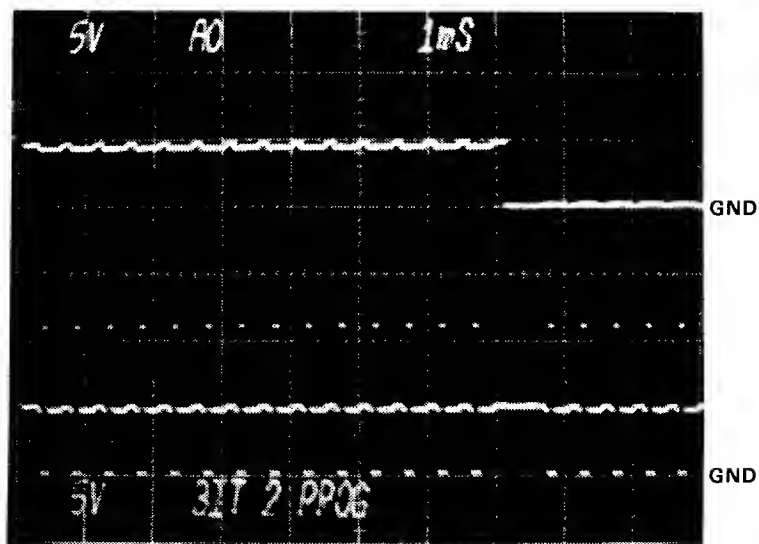
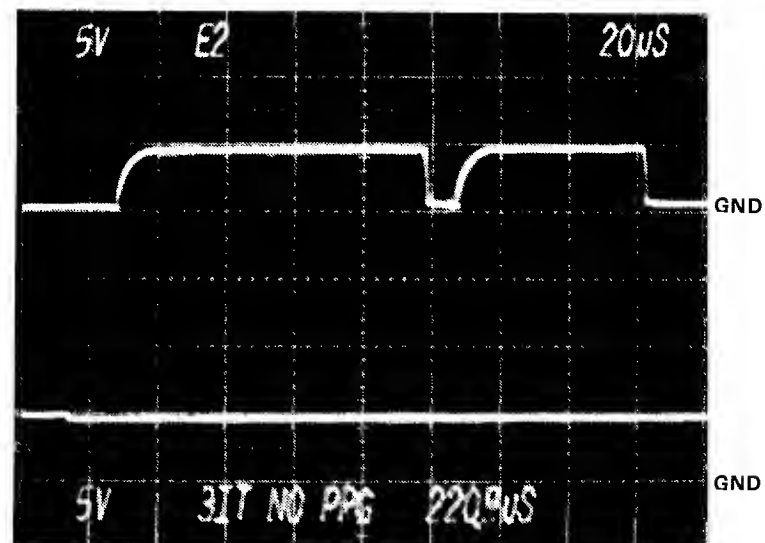
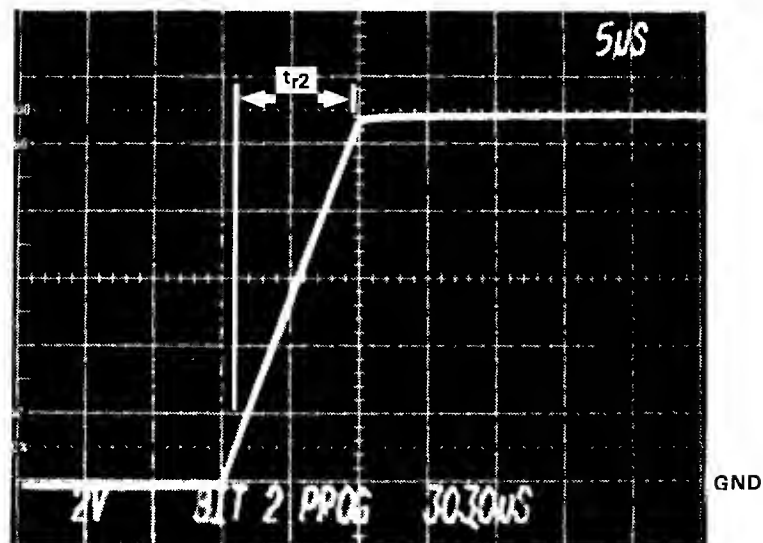
LTR	DESCRIPTION	P.E.	DATE
A	Release	R88	5/25/83

TIMING DIAGRAM

FAMILY CODE 08

Sheet 1 of 2

# DATA I/O



REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

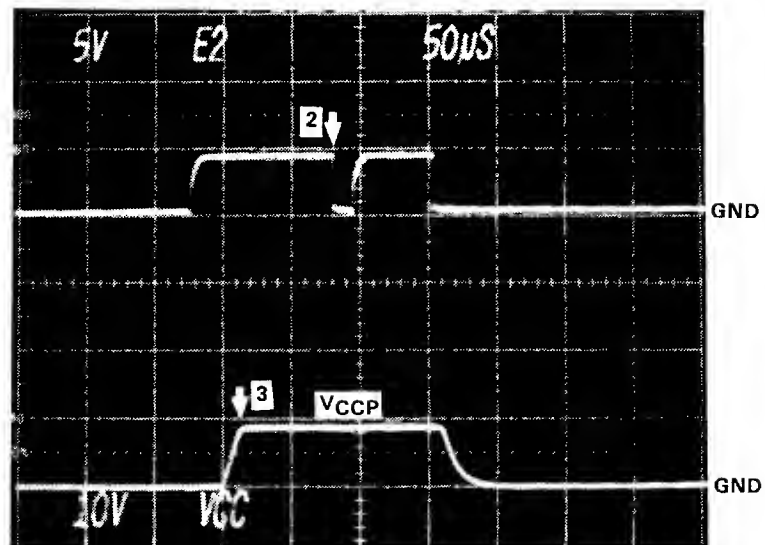
TIMING DIAGRAM

FAMILY CODE 08

Sheet 2 of 2

**DATA I/O**

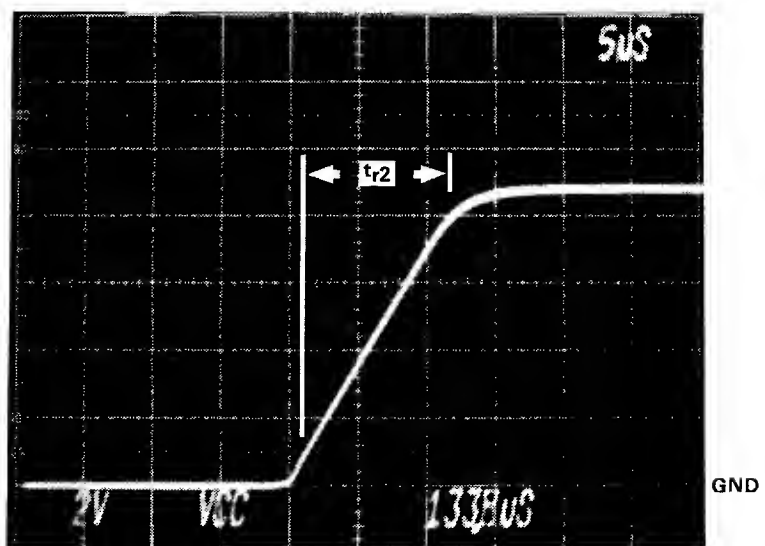




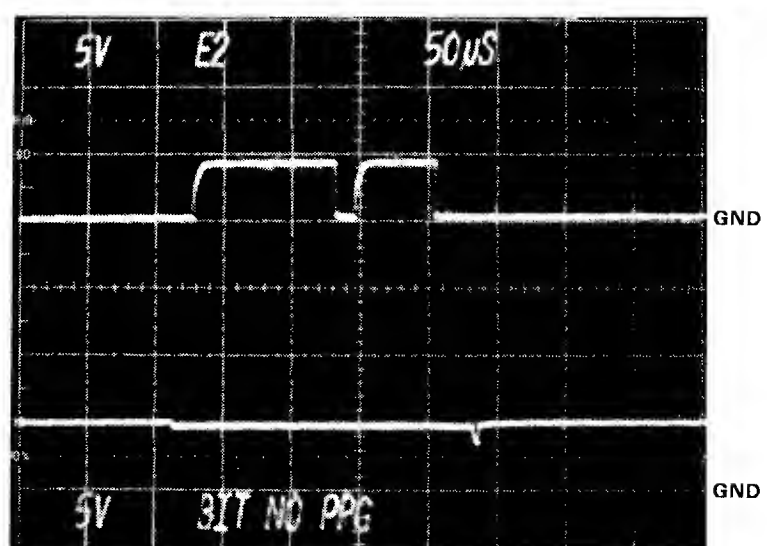
1



2



3



4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	8.5		9.0	V	
	V <sub>OP</sub>	16.5	17.0	17.5	V	
	t <sub>pw</sub>	10		15	μs	
	t <sub>r1</sub>	15		20	μs	
	t <sub>r2</sub>	5		30	μs	See note 2
	t <sub>f</sub>	0.2		10	μs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.4	4.5	4.6	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0	0	0.4	V	702-1775/TP15
	Low Load	3.5	3.8	4.2	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.4	5.5	5.6	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0	0	0.4		702-1775/TP15
	Low Load	3.5	3.8	4.2		702-1775/TP14

## NOTES

1. Load RAM with \$01.
2. Load V<sub>CC</sub> with a 330 Ω ½ watt resistor.

## REVISIONS

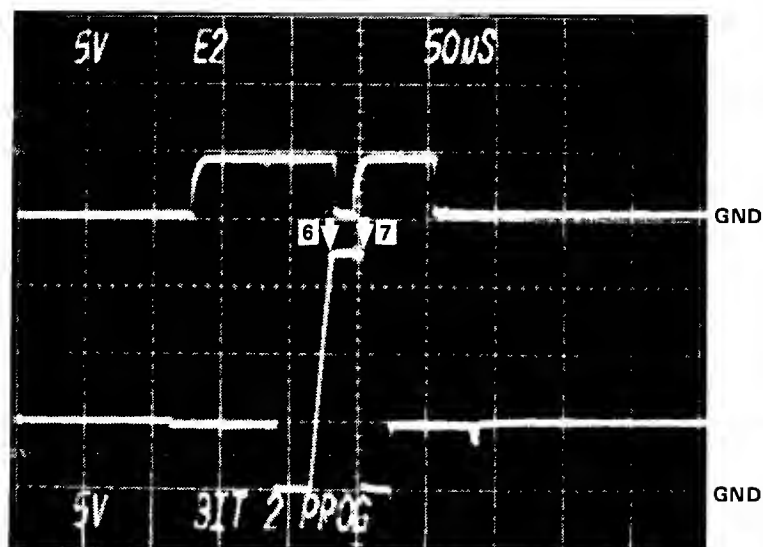
LTR	DESCRIPTION	P.E.	DATE
A	Release	R23	5/25/83

TIMING DIAGRAM

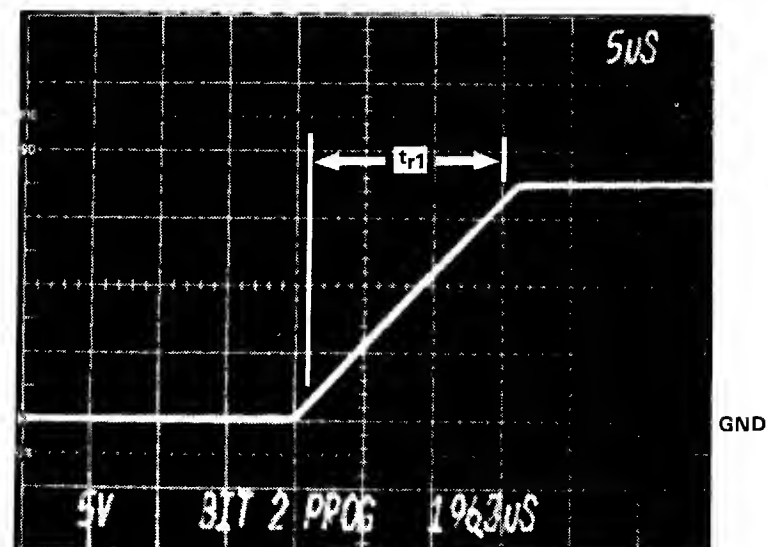
FAMILY CODE 10

Sheet 1 of 2

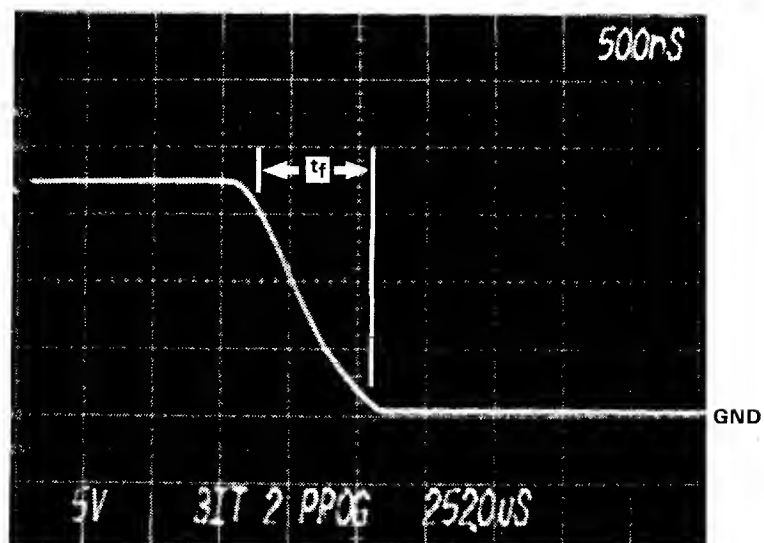
# DATA I/O



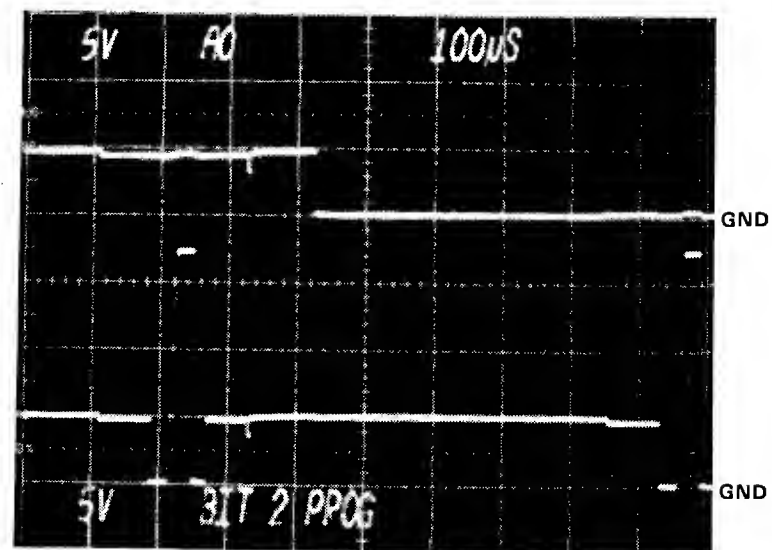
5



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7



8

REVISIONS

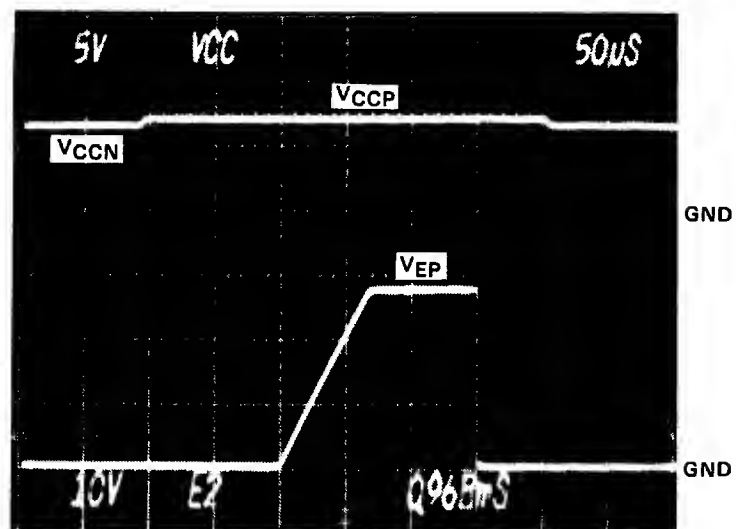
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

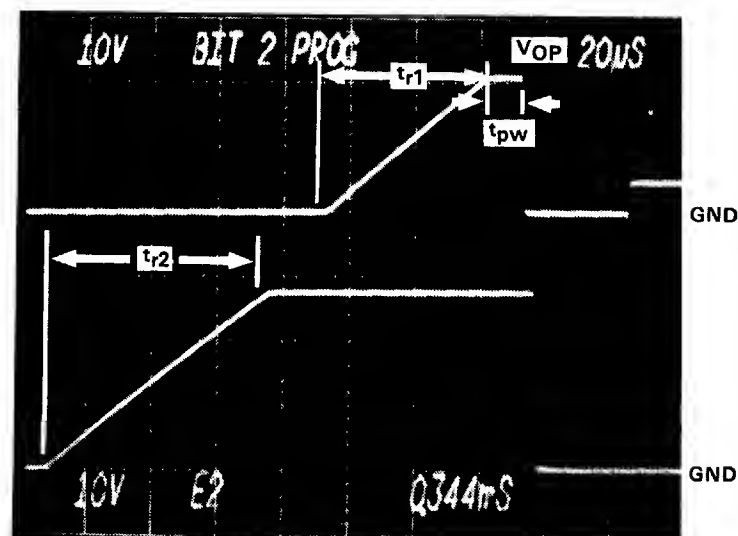
FAMILY CODE 10

Sheet 2 of 2

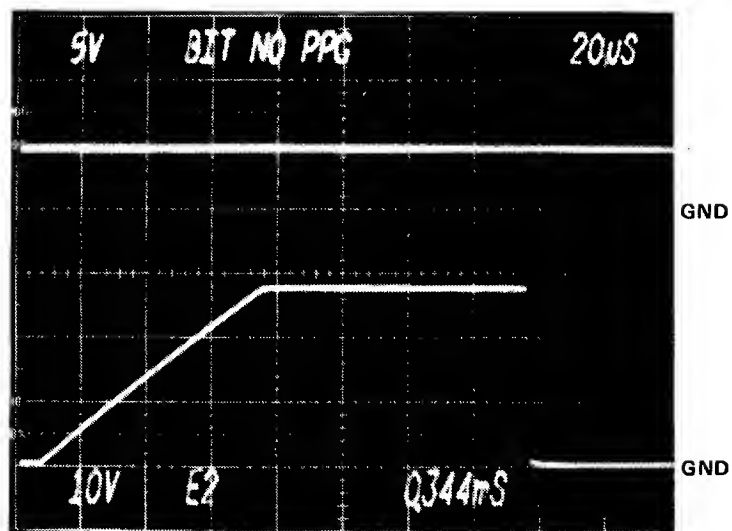
**DATA I/O**



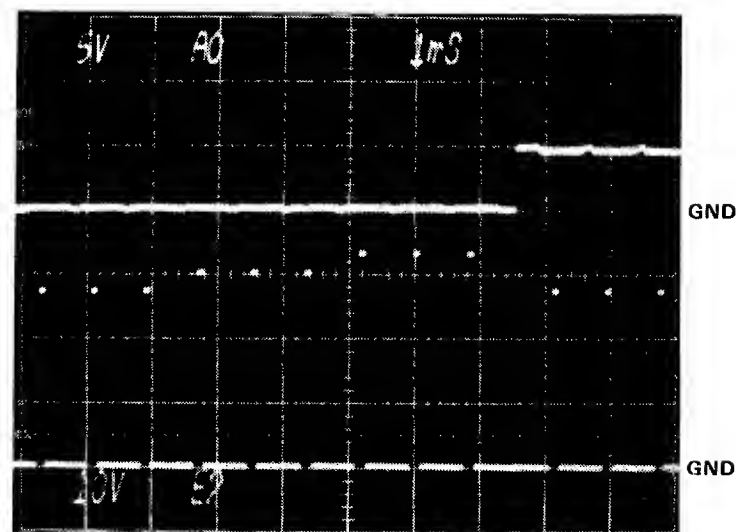
1



2



3



4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.4	5.5	5.6	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	18	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	V <sub>EP</sub>	28	27	28	V	Pulses 1-3
		29	30	31	V	Pulses 4-6
		32	33	34	V	Pulses 7-9
	t <sub>pw</sub>	10		40	μs	
	t <sub>r2</sub>	53	66	88	μs	See note 2
	t <sub>r1</sub>	42	52	69	μs	See note 2
	t <sub>f</sub>					NA
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.1	4.2	4.3	V	
	V <sub>REF</sub>	0.8	0.9	1.0	V	702-1775/TP18
	High Load	13.4	13.7	14.1	V	702-1775/TP15
	Low Load	13.4	13.7	14.1	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	5.9	6.0	6.1	V	
	V <sub>REF</sub>	2.9	3.0	3.1	V	702-1775/TP18
	High Load	0	0	0.4		702-1775/TP15
	Low Load	7.1	7.5	7.9		702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. This is measured from 10% to 90% on the tallest pulse.

## REVISIONS

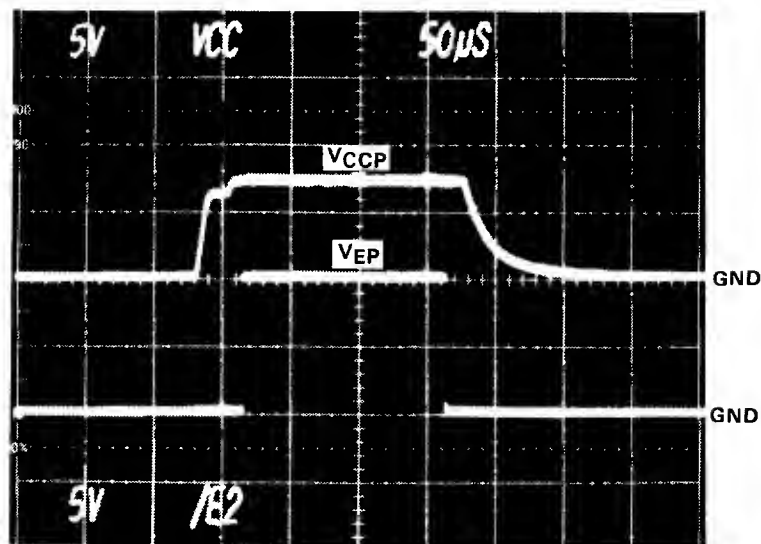
LTR	DESCRIPTION	P.E.	DATE
A	Release	RJR	5/25/93

TIMING DIAGRAM

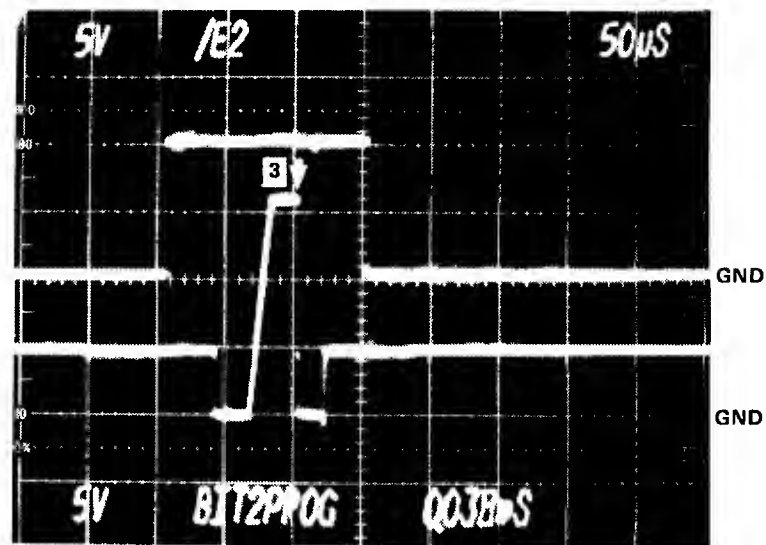
FAMILY CODE 11

Sheet 1 of 1

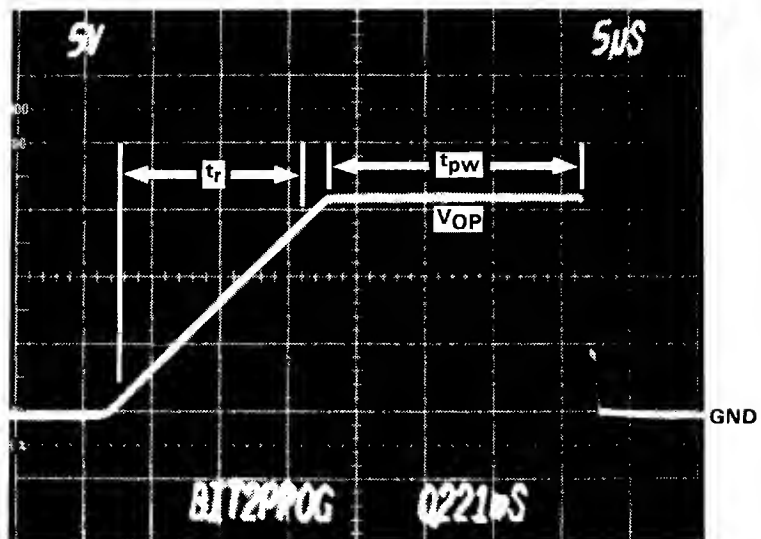
# DATA I/O



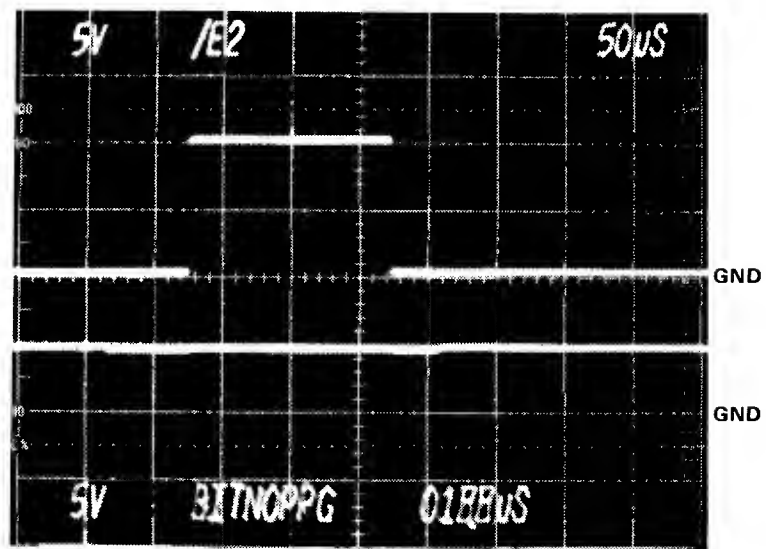
1



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4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.75	6.0	6.25	V	NA
	V <sub>OP</sub>	15.75	16	16.25	V	
	V <sub>EP</sub>	9.75	10	11.0	V	
	t <sub>pw</sub>	15		20	μs	
	t <sub>r</sub>	10	15	20	μs	
	t <sub>f</sub>					
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS	V <sub>CC</sub>	4.4	4.5	4.6	V	
VERIFY	V <sub>REF</sub>	0.9	1.0	1.1	V	702-1775/TP18
	High Load	12.5	12.8	13.2	V	702-1775/TP15
	Low Load	12.5	12.8	13.2	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.4	5.5	5.6	V	
VERIFY	V <sub>REF</sub>	2.9	3.0	3.1	V	702-1775/TP18
	High Load	0	0	0.4		702-1775/TP15
	Low Load	9.9	10.3	10.7		702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. Photo 6 is for registered devices.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RJS	5/25/83

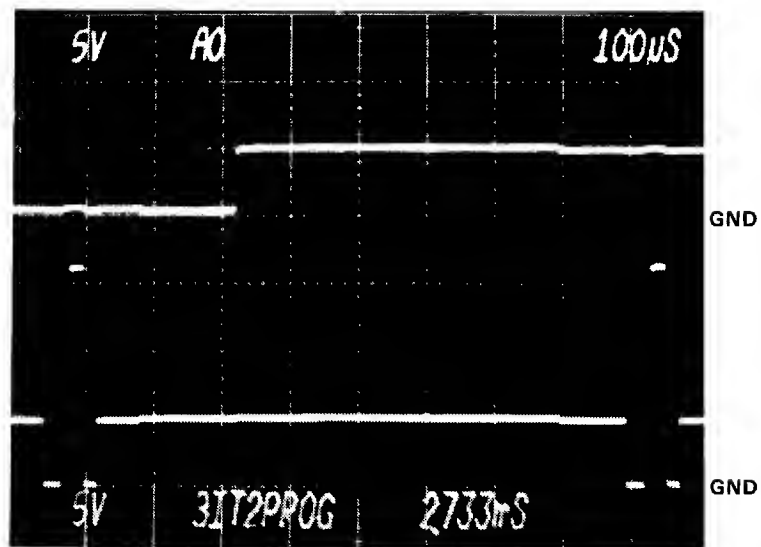
TIMING DIAGRAM

FAMILY CODE 13

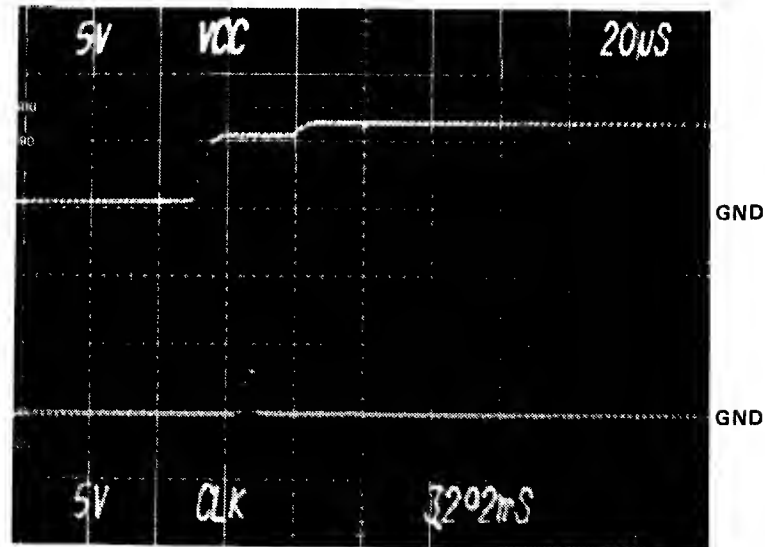
Sheet 1 of 2

# DATA I/O





5



6

# REVISIONS

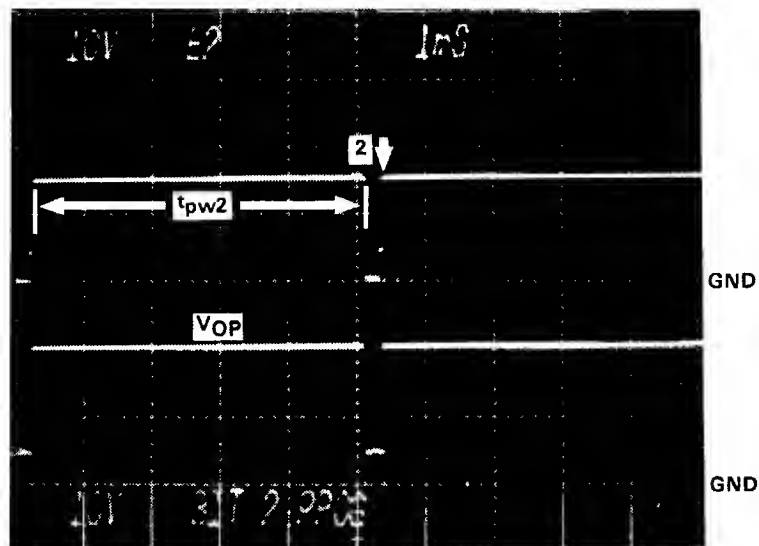
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

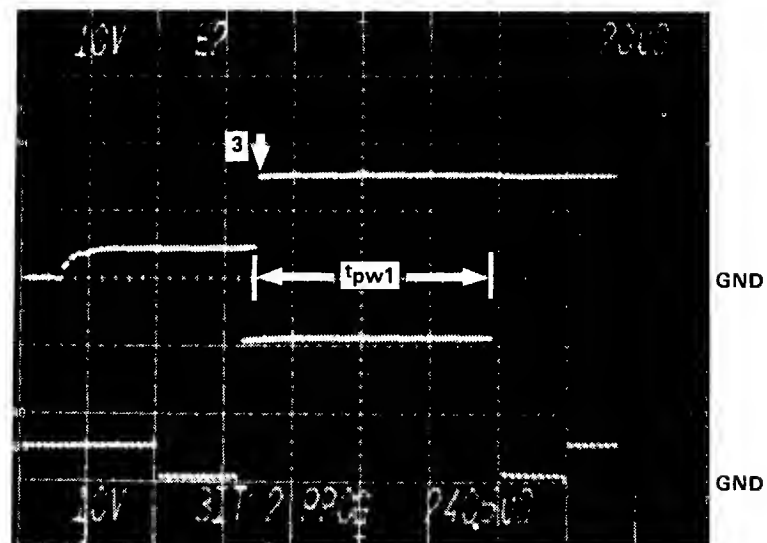
FAMILY CODE 13

Sheet 2 of 2

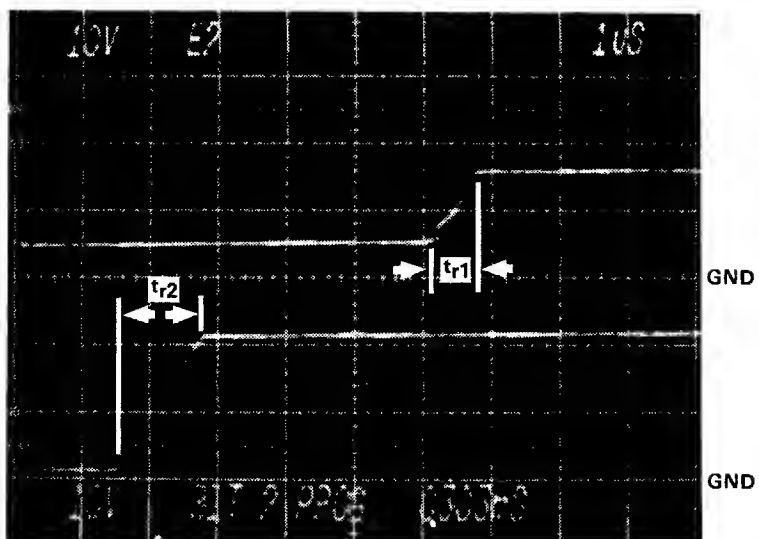
**DATA I/O**



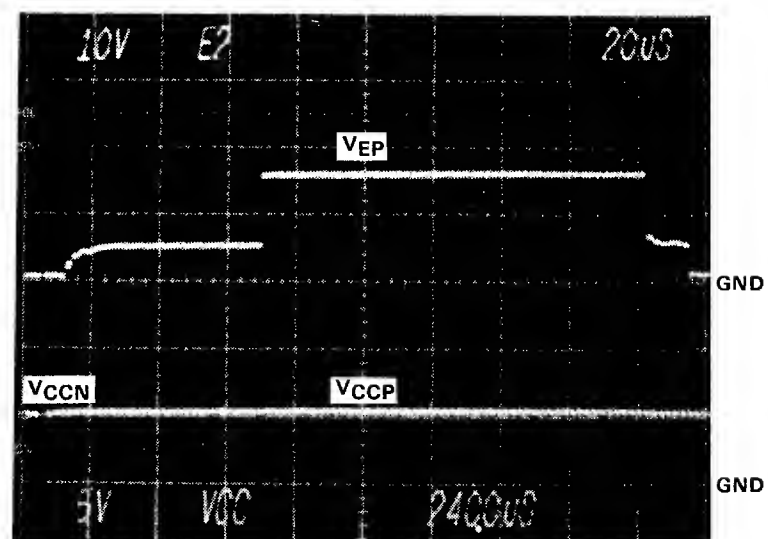
1



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4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.0	5.25	5.5	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	19.5	20.0	20.5	V	
	V <sub>EP</sub>	14.5	15.0	15.5	μs	
	T <sub>pw1</sub>	50		100	μs	Pulse 1
	T <sub>pw2</sub>	5		15	ms	Pulses 2-80
	t <sub>r1</sub>	0.2		0.7	μs	
	t <sub>r2</sub>	0.6		1.4	μs	
	t <sub>f</sub>					NA
	Reject		80		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.6	4.7	4.8	V	
VERIFY	V <sub>REF</sub>	.6	.7	.8	V	702-1775/TP18
	High Load	4.8	5.2	5.6	V	702-1775/TP15
	Low Load	4.8	5.2	5.6	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.1	5.2	5.3	V	
VERIFY	V <sub>REF</sub>	2.3	2.4	2.5	V	702-1775/TP18
	High Load	4.8	5.2	5.6	V	702-1775/TP15
	Low Load	4.8	5.2	5.6	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE for Family 15.
2. Load RAM with \$01 for Family 16.

## REVISIONS

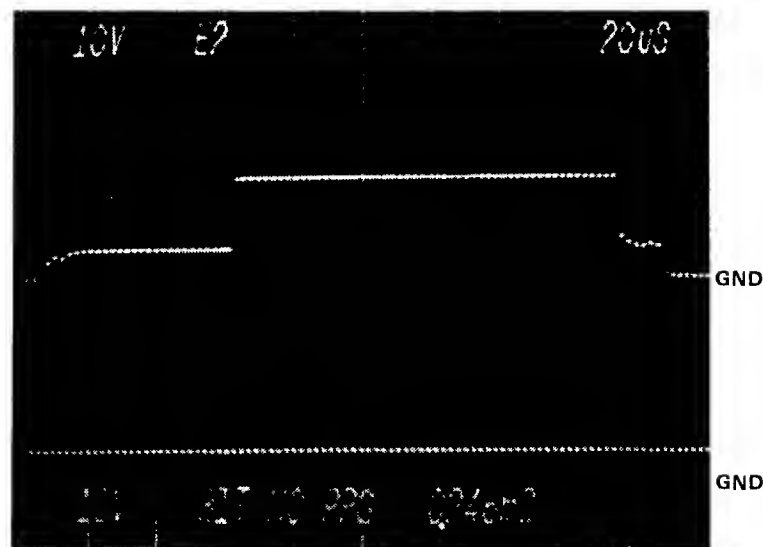
LTR	DESCRIPTION	P.E.	DATE
A	Release	RJS	5/25/83

## TIMING DIAGRAM

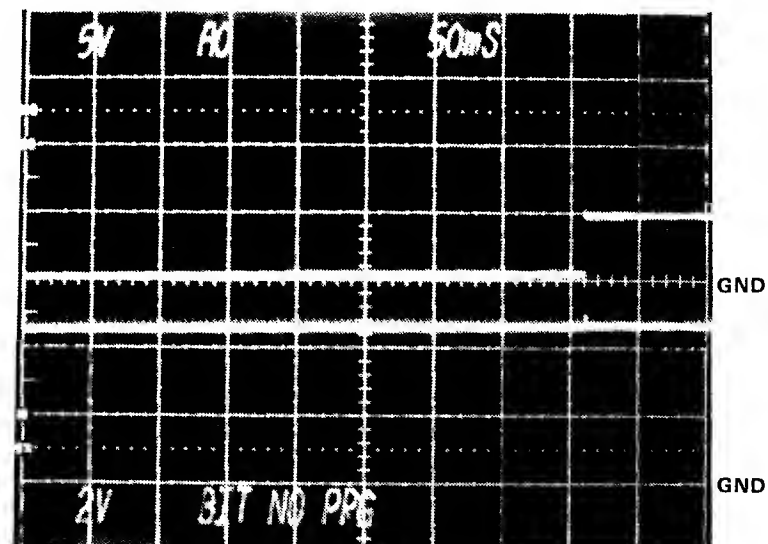
FAMILY CODE 15, 16

Sheet 1 of 2

# DATA I/O



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6

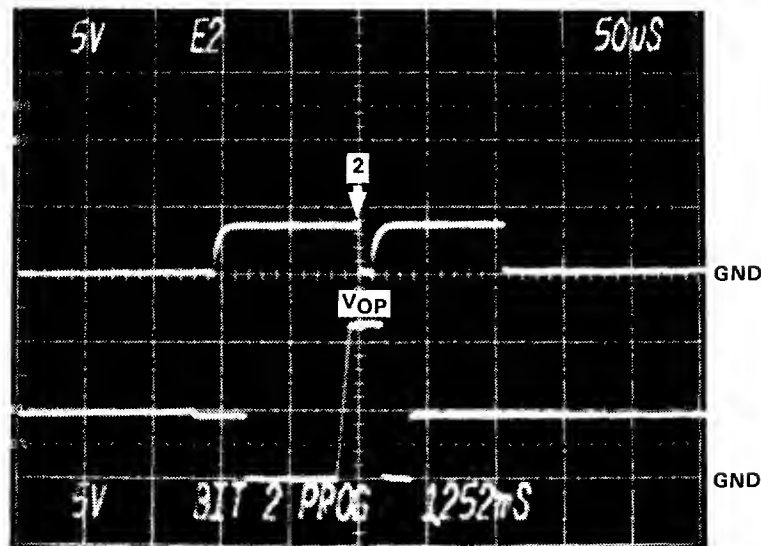
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

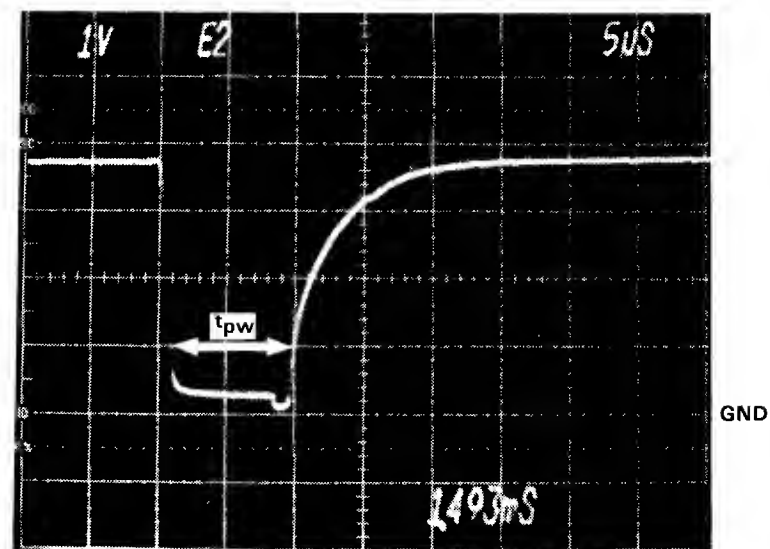
TIMING DIAGRAM  
FAMILY CODE 15, 16

Sheet 2 of 2

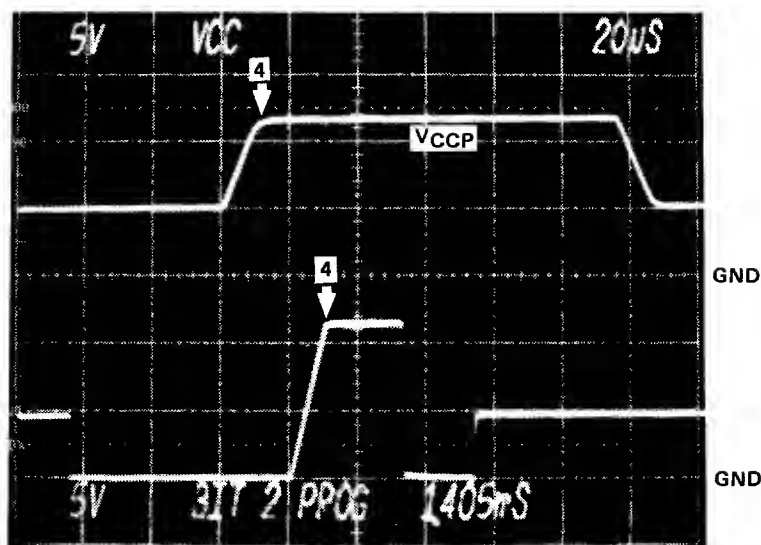
**DATA I/O**



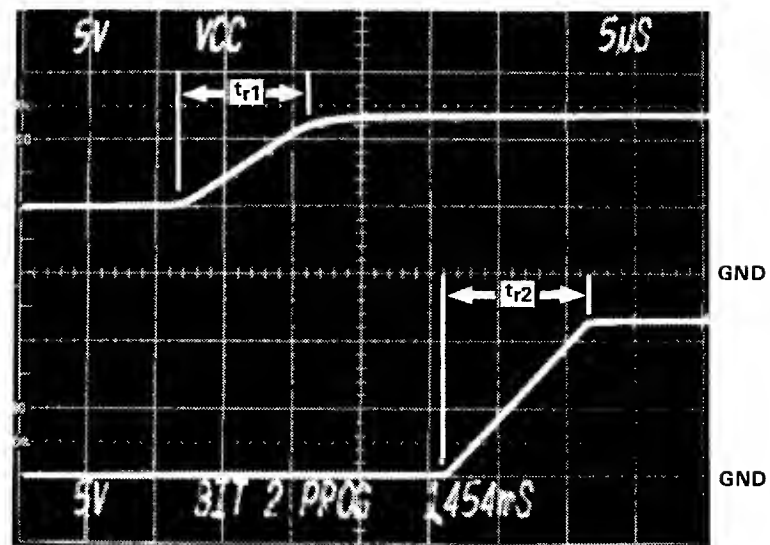
1



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4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	11.5	11.7	12.0	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	10.5	11.0	11.5	V	
	t <sub>pw</sub>	9.0	10.0	11.0	μs	
	t <sub>r1</sub>	1.0		20.0	μs	See note 2
	t <sub>r2</sub>	1.0		15.0	μs	
	t <sub>f</sub>					NA
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS	V <sub>CC</sub>	4.2	4.3	4.4	V	
VERIFY	V <sub>REF</sub>	0.8	0.9	1.0	V	702-1775/TP18
	High Load	13.4	13.7	14.1	V	702-1775/TP15
	Low Load	13.4	13.7	14.1	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.9	6.0	6.1	V	
VERIFY	V <sub>REF</sub>	2.9	3.0	3.1	V	702-1775/TP18
	High Load	0.0	0.0	0.4	V	702-1775/TP15
	Low Load	7.1	7.5	7.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$01.
2. Load V<sub>CC</sub> with a 330 Ω ½ watt resistor.

## REVISIONS

LTR	DESCRIPTION	P. E.	DATE
A	Release	RLS	5/27/83

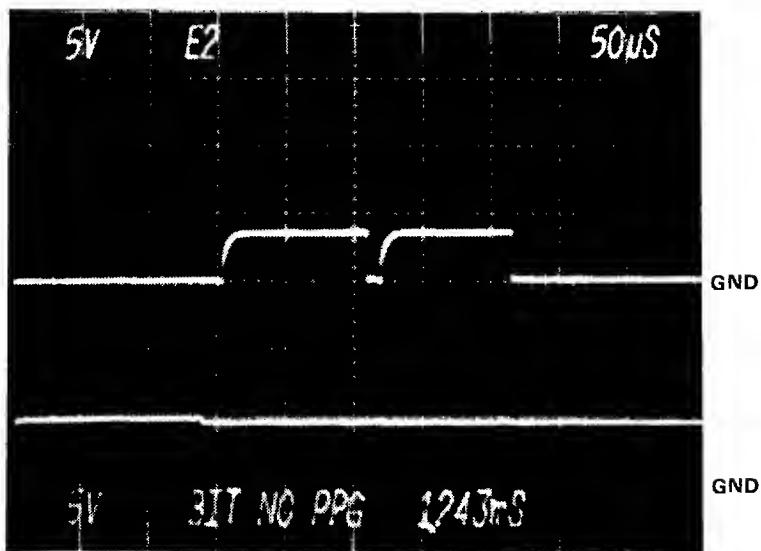
TIMING DIAGRAM

FAMILY CODE 18

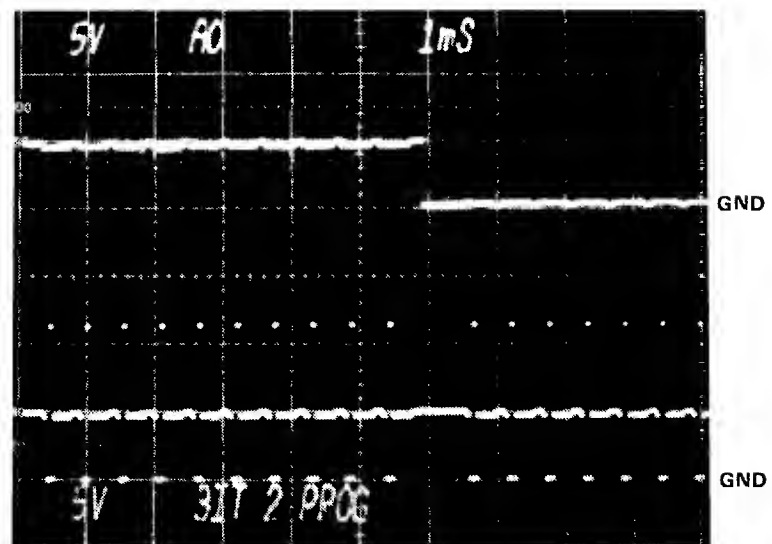
Sheet 1 of 2

# DATA I/O





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# REVISIONS

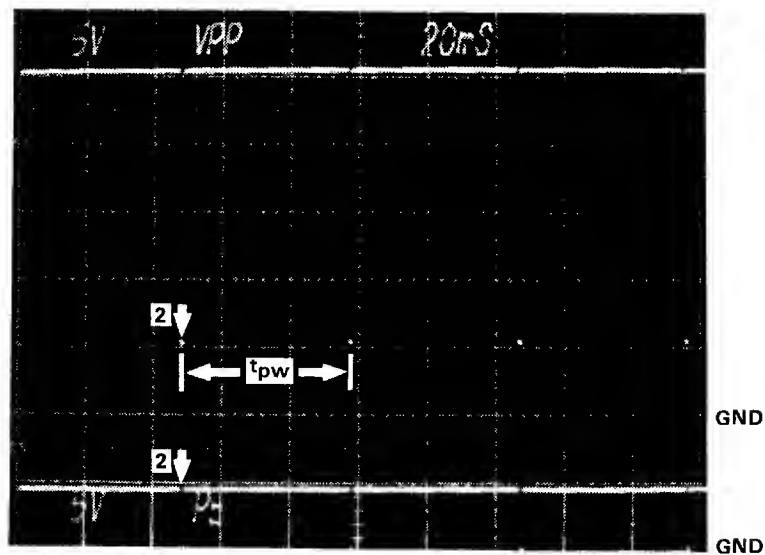
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

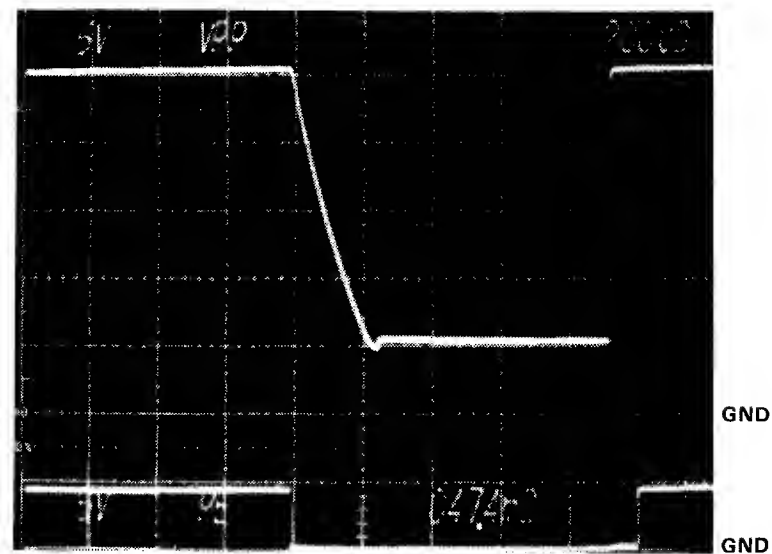
FAMILY CODE 18

Sheet 2 of 2

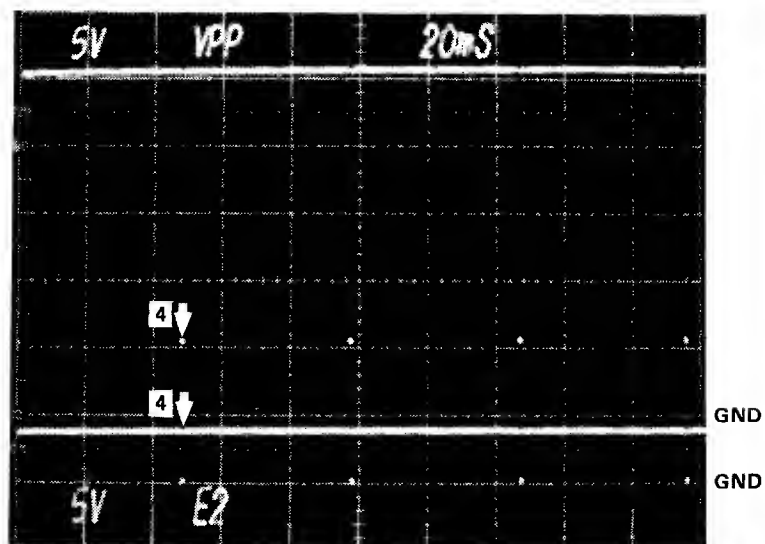
**DATA I/O**



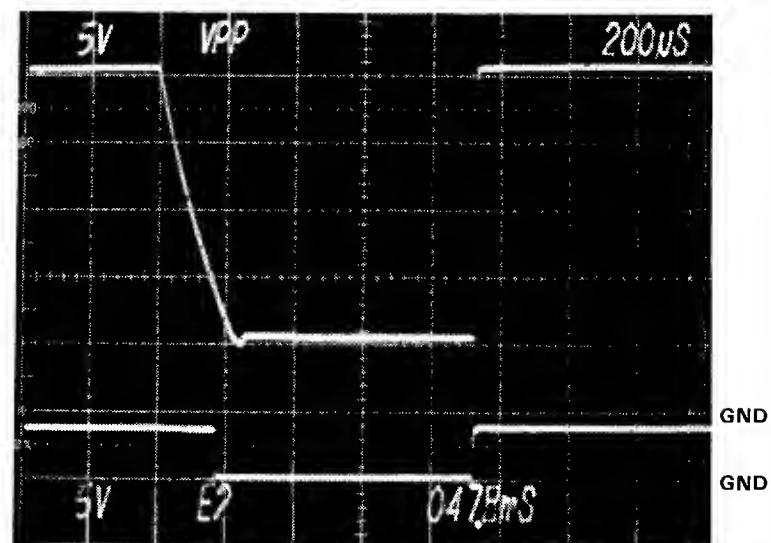
1



2



3



4

# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Pinout 24
	VOP	3.8	5.0	6.0	V	
	Vpp	24.0	25.0	26.0	V	
	Vppv	4.75	5.00	5.25	µs	
	Vppv	0.0	0.0	0.8	V	
	tpw	48	50	52	ms	
	tr	50			ns	
	tf	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
VERIFY	VREF	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	
2ND PASS	VCC	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
VERIFY	VREF	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	

# NOTES

1. Load RAM with \$FE.
2. Photos 11 and 12 are for Pinout 24.
3. Photos 13 and 14 are for Pinout 25.
4. Photo 15 is for Pinout 49 using the same set-up as photo 12.
5. Photo 16 is for Pinout 50, using the same set-up as photo 14.

# REVISIONS

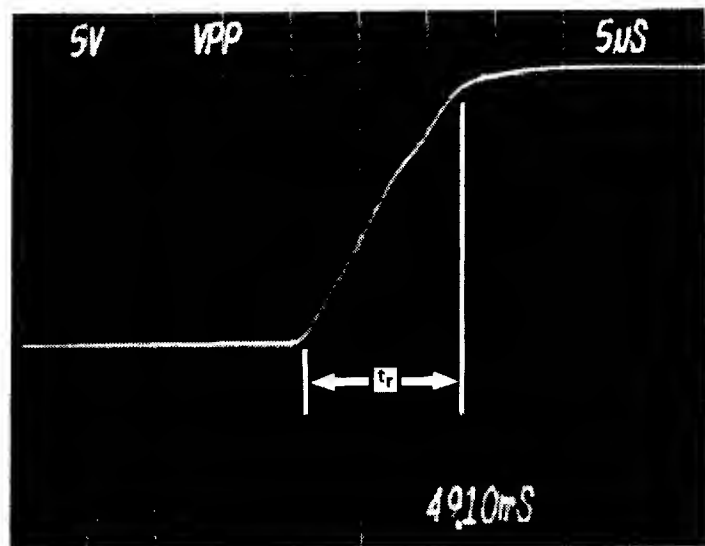
LTR	DESCRIPTION	P. E.	DATE
A	Release	123	5/25/83

TIMING DIAGRAM

FAMILY CODE 19

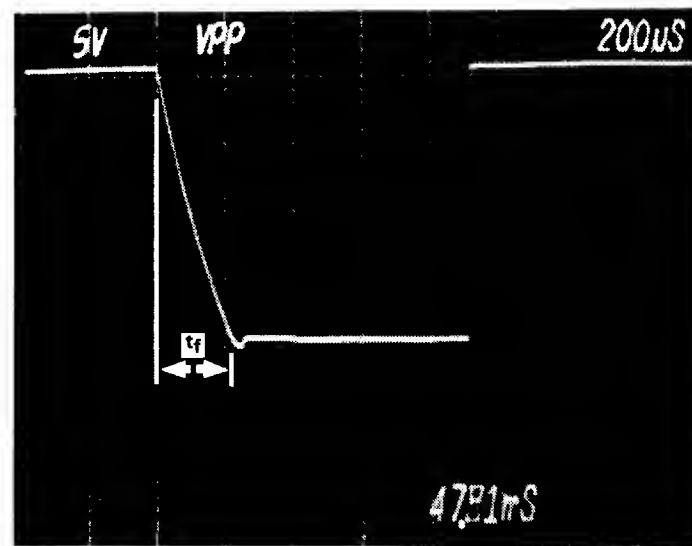
Sheet 1 of 4

**DATA I/O**



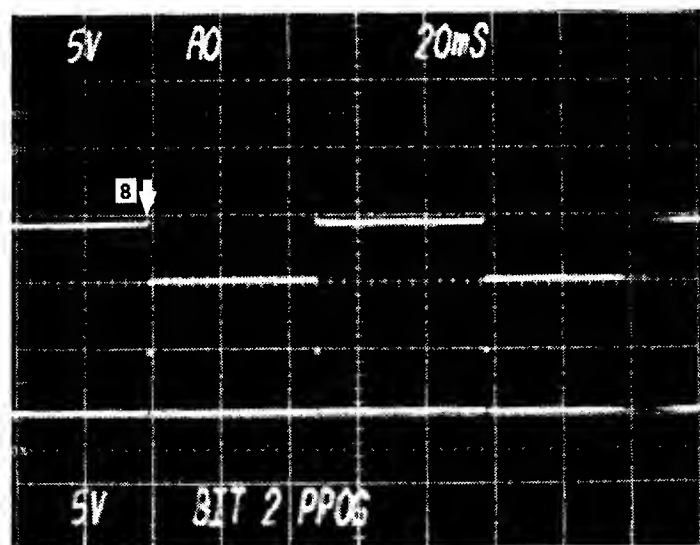
GND

5



GND

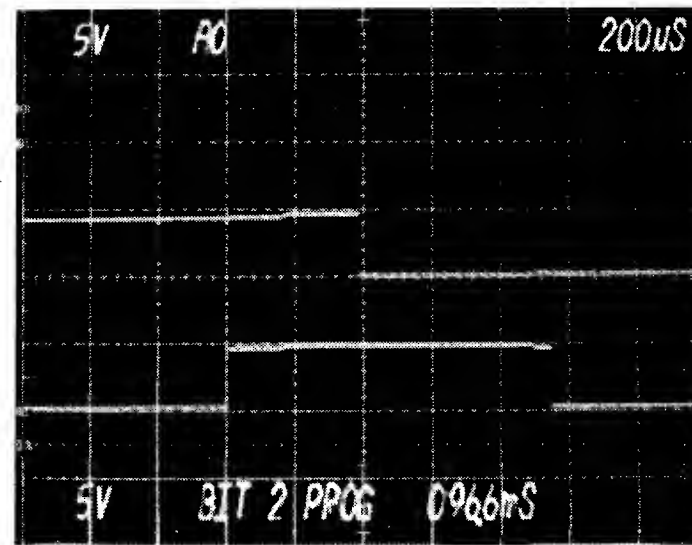
6



GND

GND

7



GND

GND

8

REVISIONS

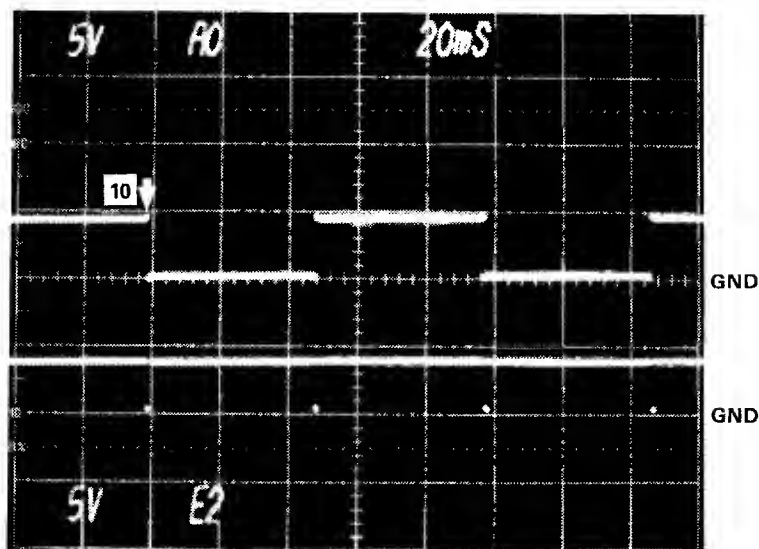
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

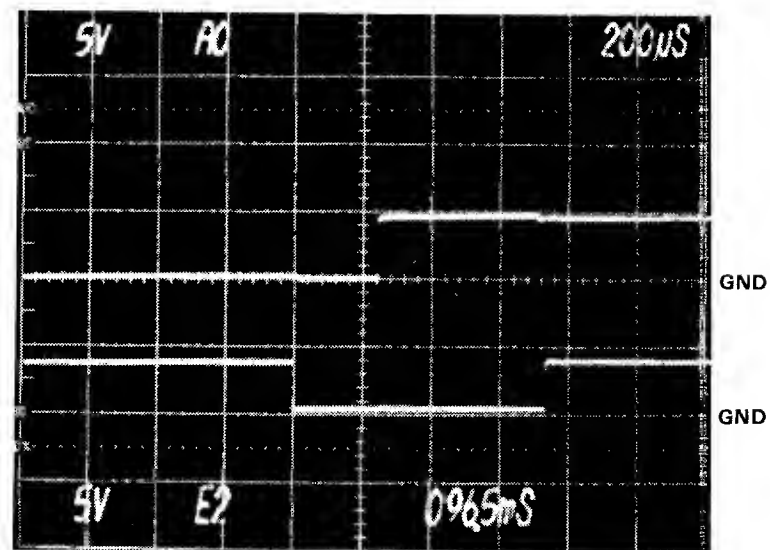
FAMILY CODE 19

Sheet 2 of 4

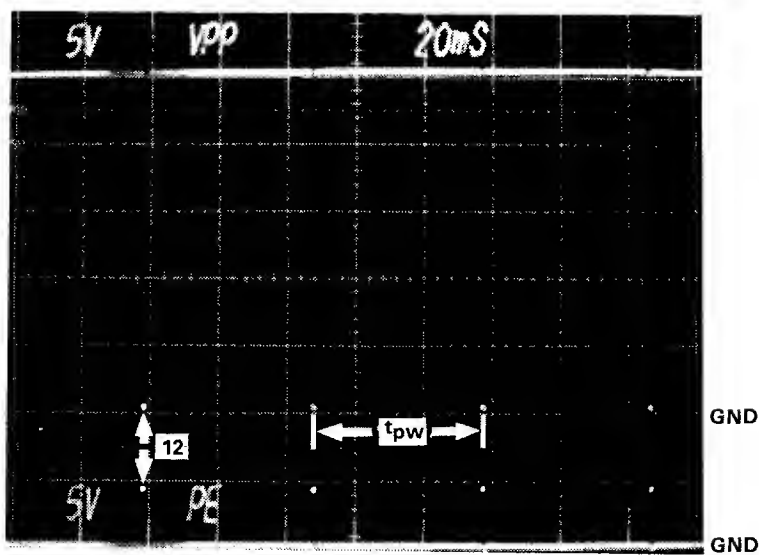
**DATA I/O**



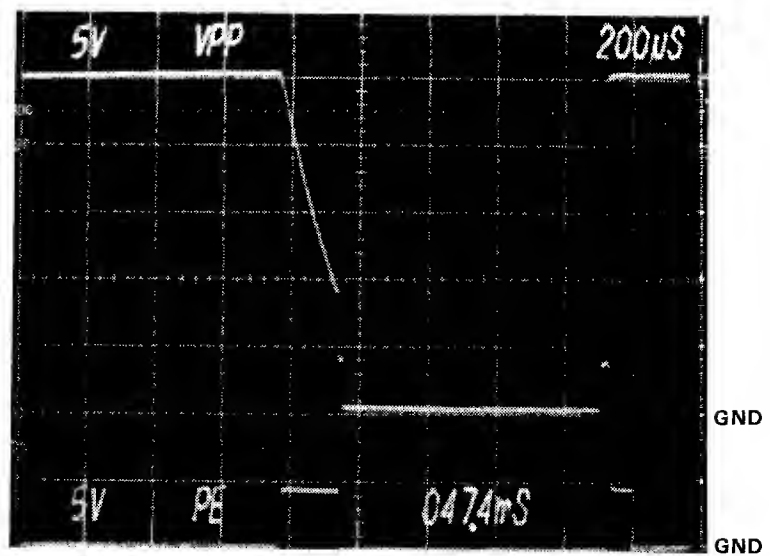
9



10



11



12

# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

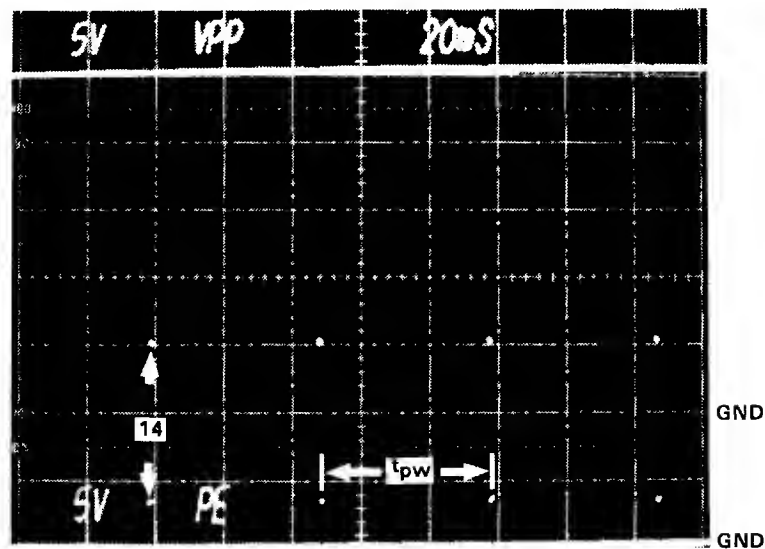
TIMING DIAGRAM

FAMILY CODE 19

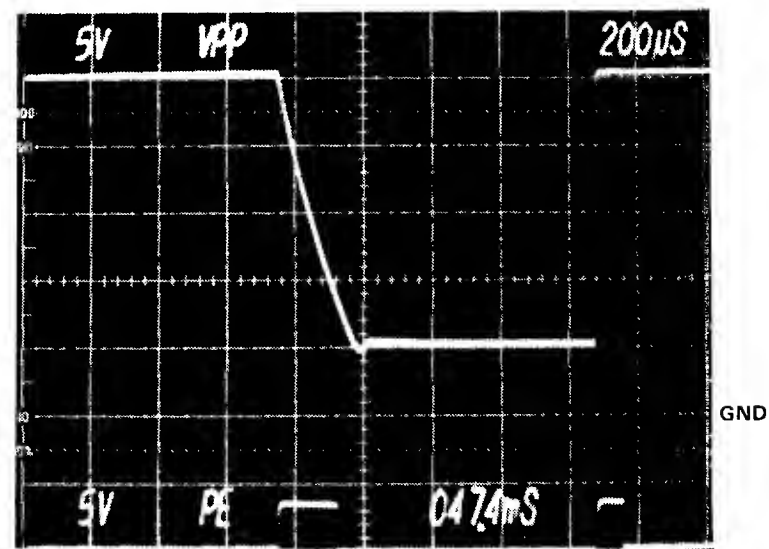
Sheet 3 of 4

**DATA I/O**

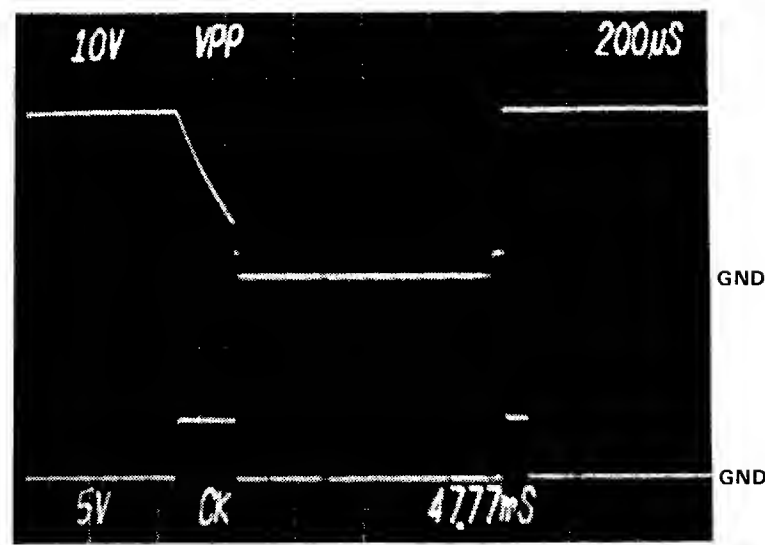




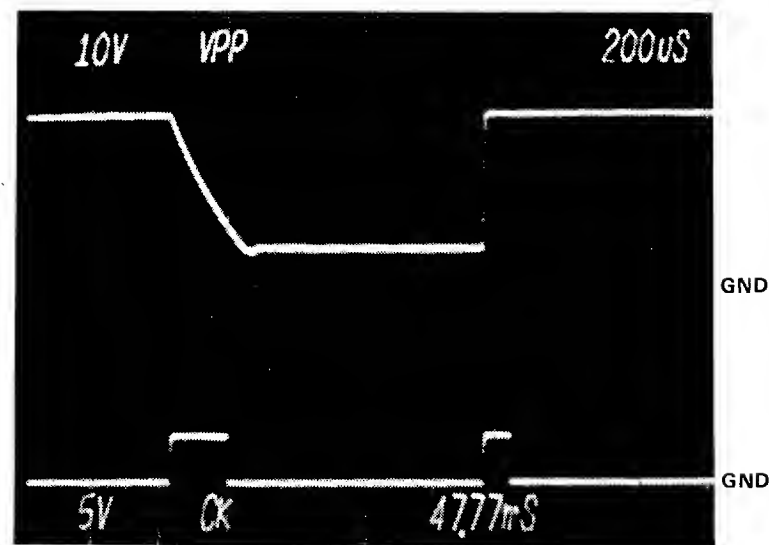
13



14



15



16

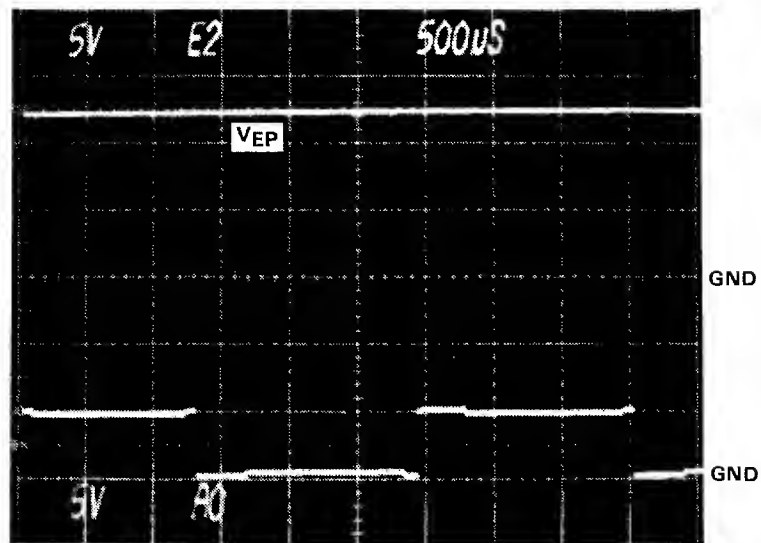
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

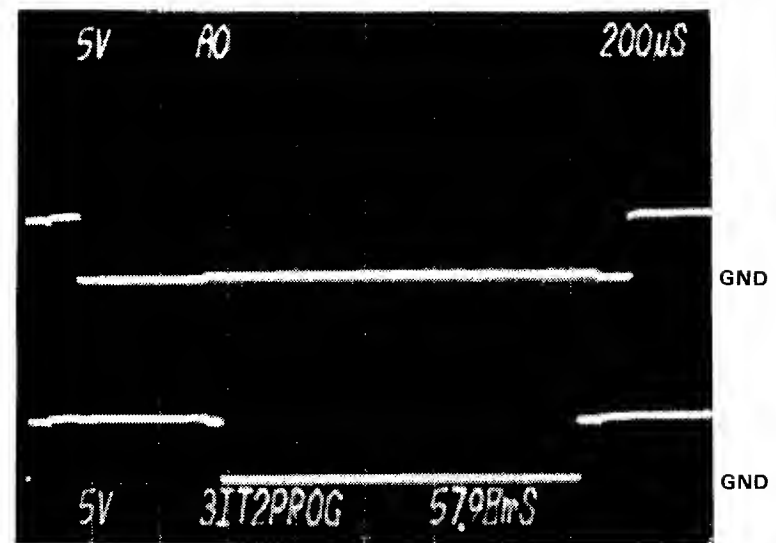
TIMING DIAGRAM

FAMILY CODE 19

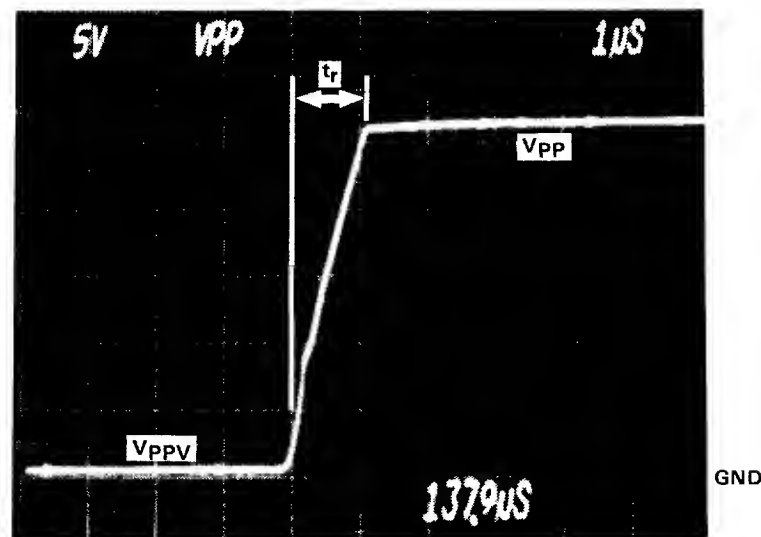
**DATA I/O**



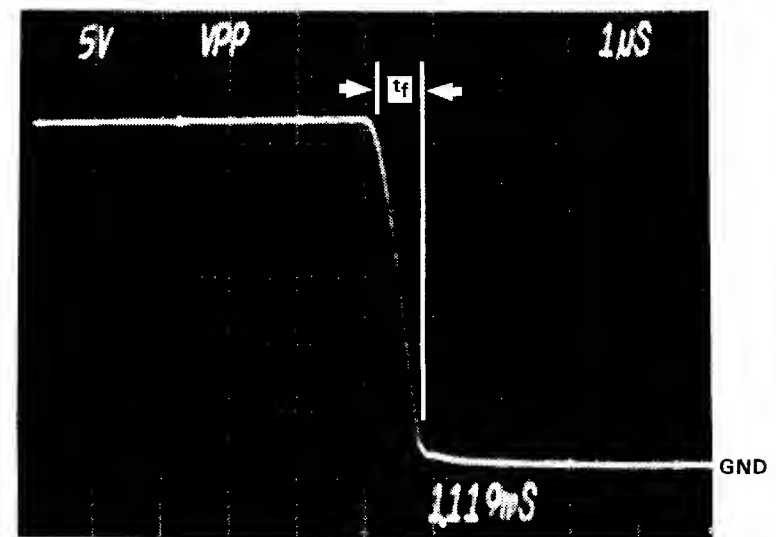
1



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3



4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	
	V <sub>OP</sub>	3.8	5.0	6.0	V	
	V <sub>PP</sub>	25.0	26.0	27.0	V	
	V <sub>PPV</sub>	0.0	0.0	1.0	V	
	V <sub>EP</sub>	11.4	12.0	12.6	V	
	V <sub>BB</sub>	-5.25	-5.00	-4.75	V	Not Shown
	V <sub>DD</sub>	11.4	12.0	12.6	V	Not Shown
	t <sub>pw</sub>	0.8	1.0	1.2	ms	
	t <sub>r</sub>	0.5	1.0	2.0	μs	
	t <sub>f</sub>	0.5	1.0	2.0	μs	
	Reject		100		Loops	See note 2
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address.

## REVISIONS

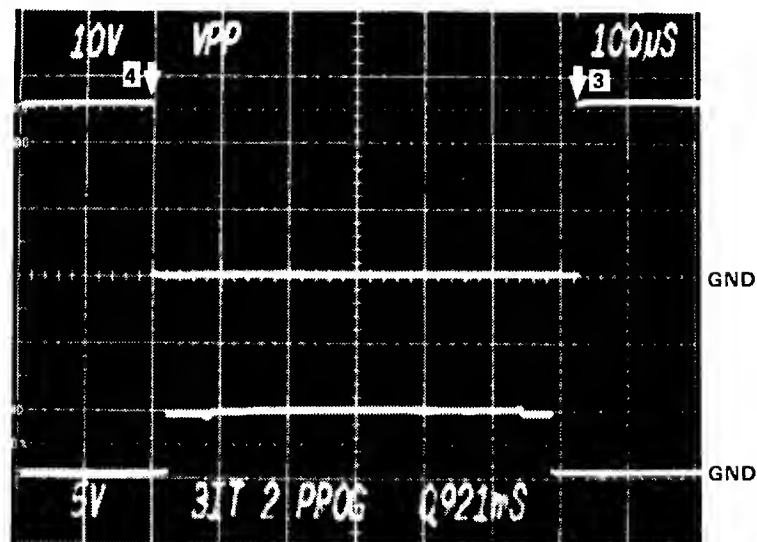
LTR	DESCRIPTION	P.E.	DATE
A	Release	R28	5/25/03

TIMING DIAGRAM

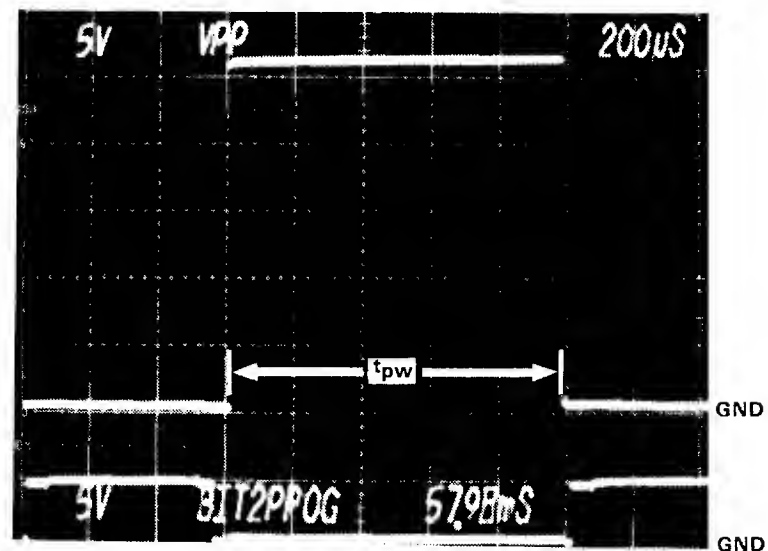
FAMILY CODE 21

Sheet 1 of 2

# DATA I/O



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# REVISIONS

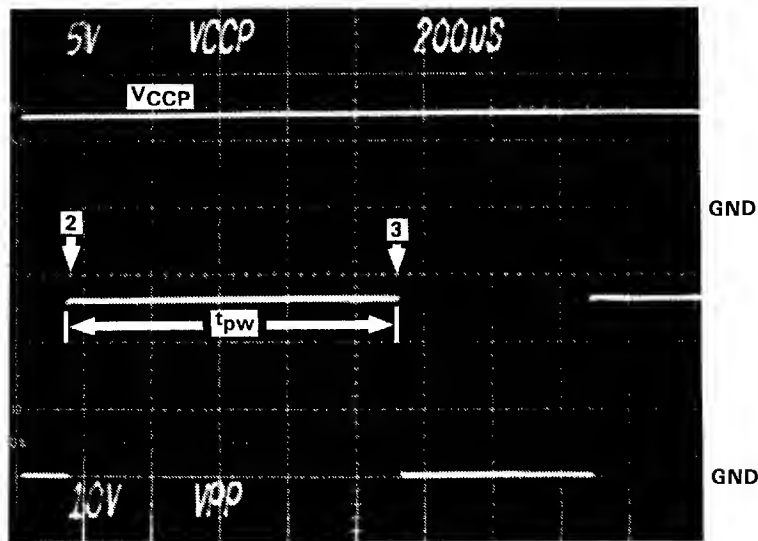
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

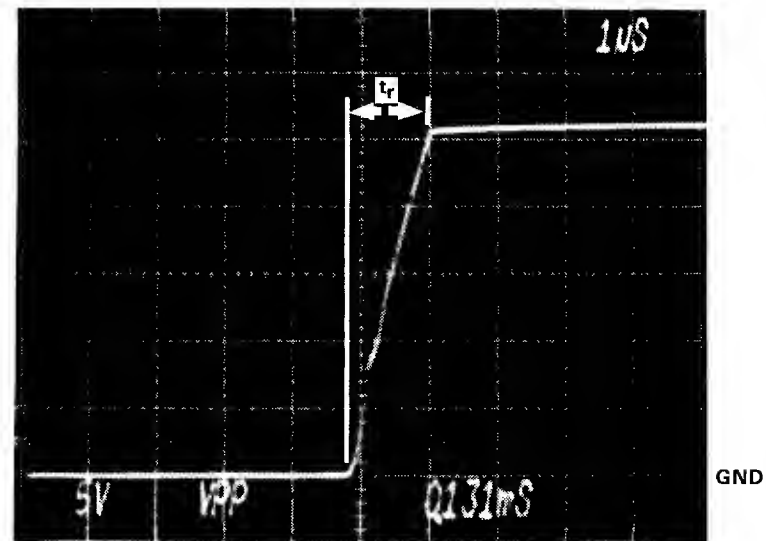
FAMILY CODE 21

Sheet 2 of 2

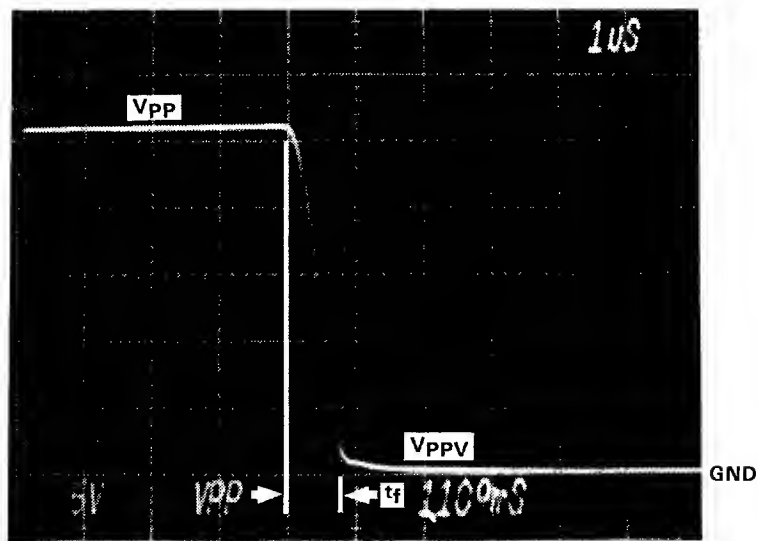
**DATA I/O**



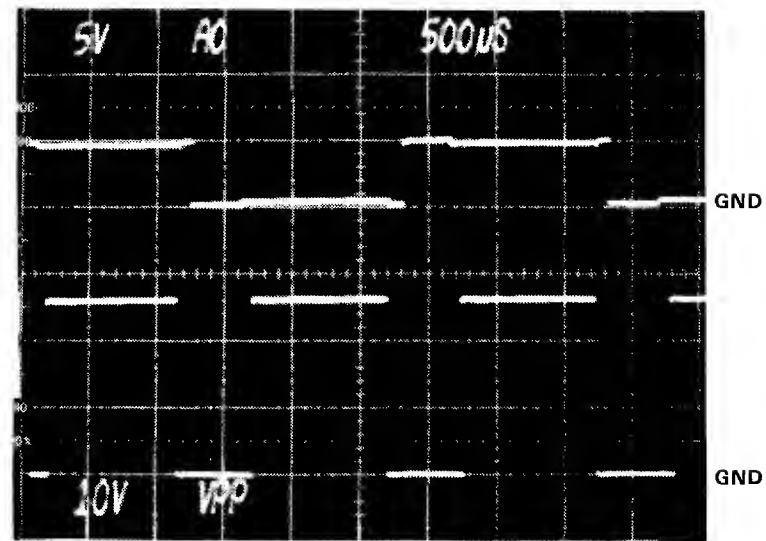
1



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4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	11.4	12.0	12.6	V	NA
	V <sub>OP</sub>					
	V <sub>PP</sub>	25.0	26.0	27.0	V	
	V <sub>PPV</sub>	0.0		1.0	V	
	V <sub>88</sub>	-5.25	-5.0	-4.75	V	Not Shown
	V <sub>DD</sub>	11.4	12.0	12.4	V	Not Shown
	t <sub>pw</sub>	0.8	1.0	1.2	ms	
	t <sub>r</sub>	0.5		2.0	μs	
	t <sub>f</sub>	0.5		2.0	μs	
	Reject Overprogram		100 0		Loops Pulses	See note 2
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. All 100 loops are performed, and the device is read and verified after all 100 loops.

## REVISIONS

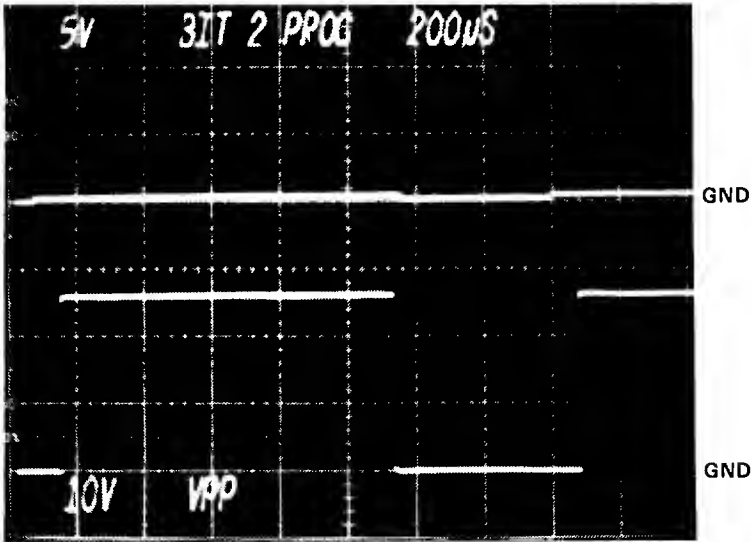
LTR	DESCRIPTION	P.E.	DATE
A	Release	R23	5/25/83

TIMING DIAGRAM

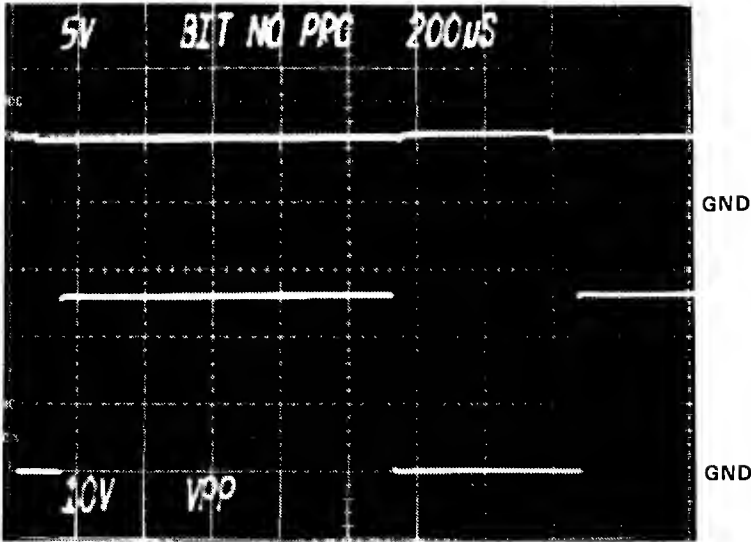
FAMILY CODE 23

Sheet 1 of 2 **DATA I/O**





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# REVISIONS

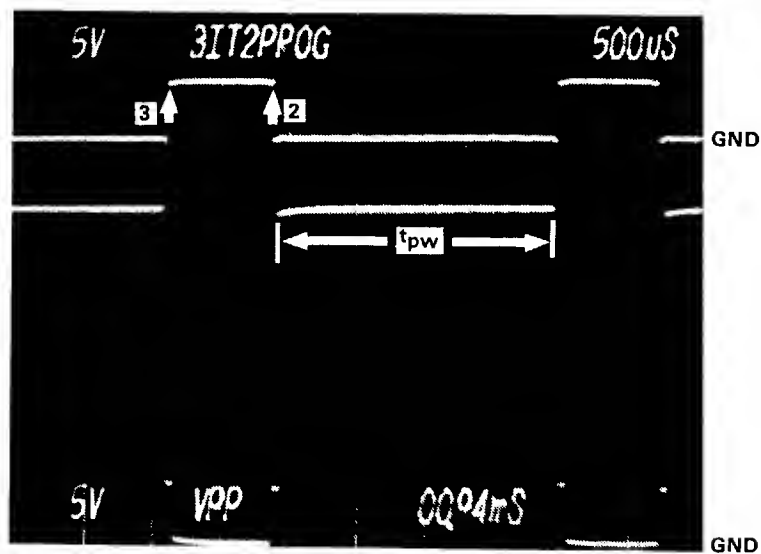
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

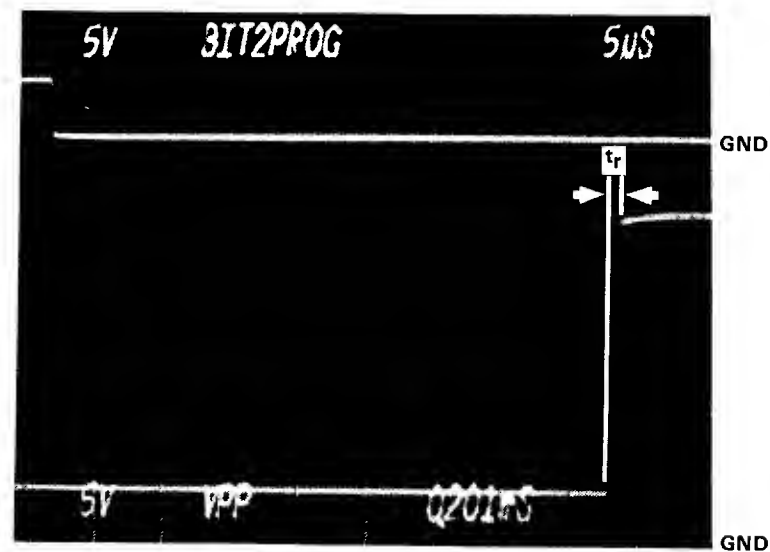
FAMILY CODE 23

Sheet 2 of 2

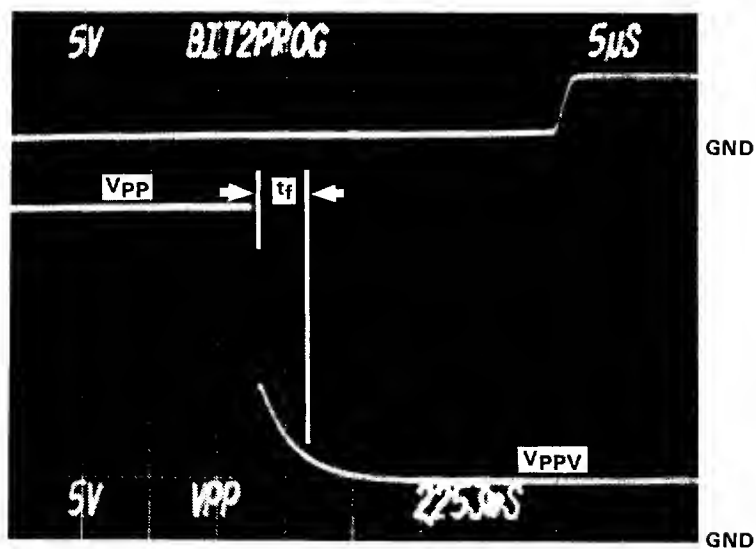
**DATA I/O**



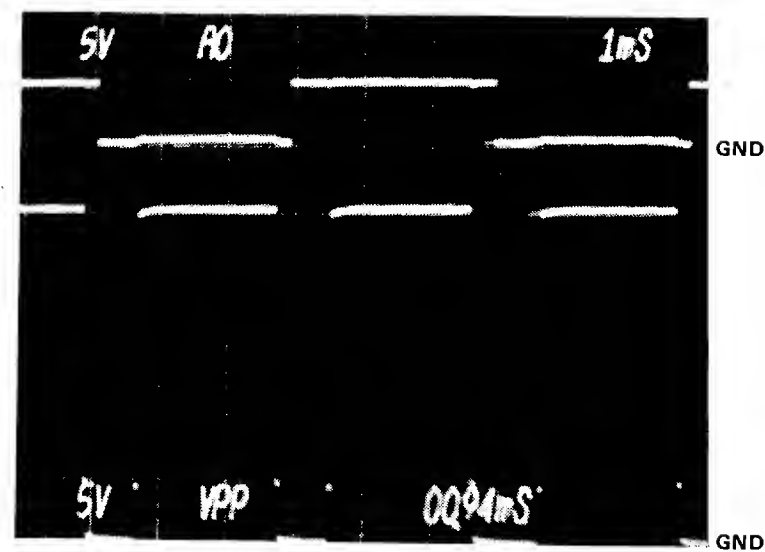
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not Shown
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	24.0	25.0	26.0	V	
	V <sub>PPV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	1.9	2.0	2.1	ms	
	t <sub>r</sub>	0.5		2.0	μs	
	t <sub>f</sub>	0.5		5.0	μs	
	Reject		20		Loops	See note 2
	Overprogram		5		Loops	See note 2
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. A read and verify is done after each loop, and when the device verifies, 5 more loops are applied.

## REVISIONS

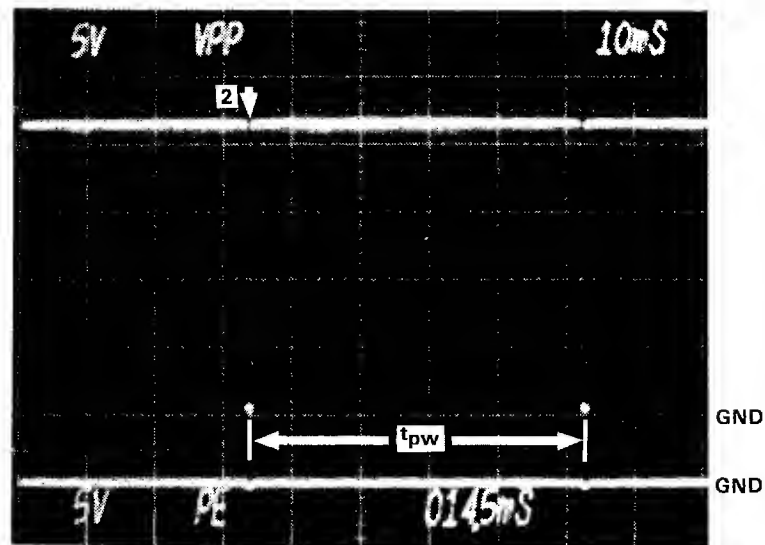
LTR	DESCRIPTION	P.E.	DATE
A	Release	R22	5/25/83

TIMING DIAGRAM

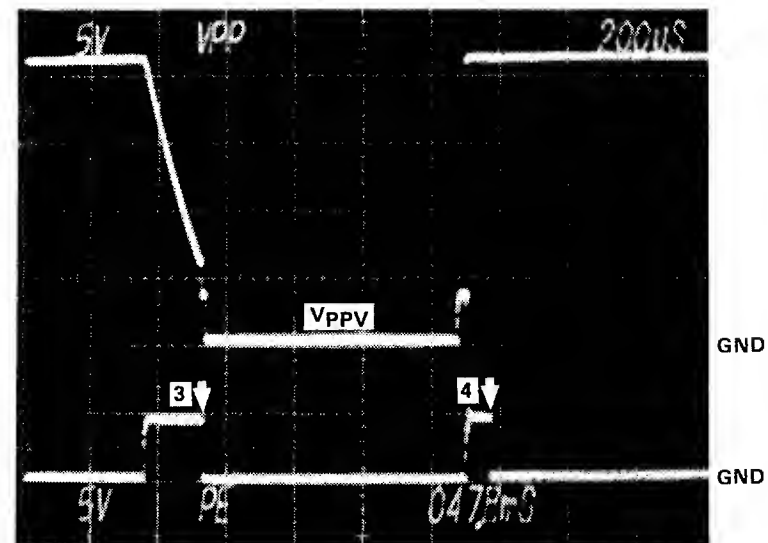
FAMILY CODE 25

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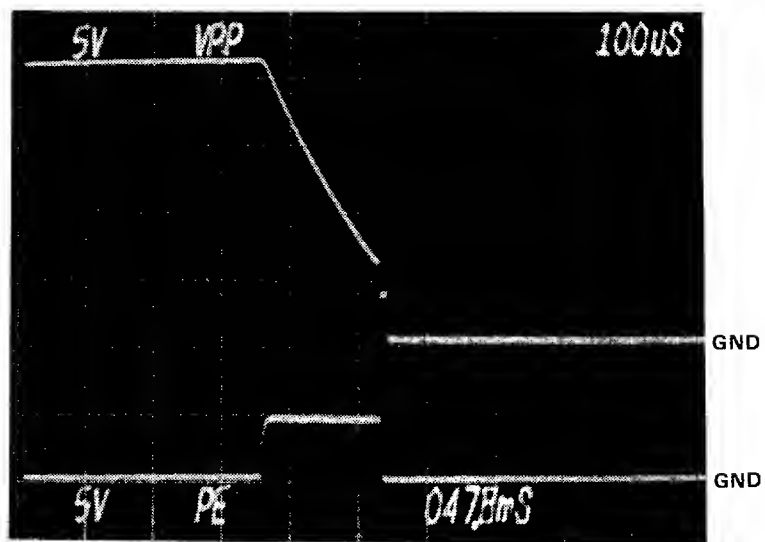
# DATA I/O



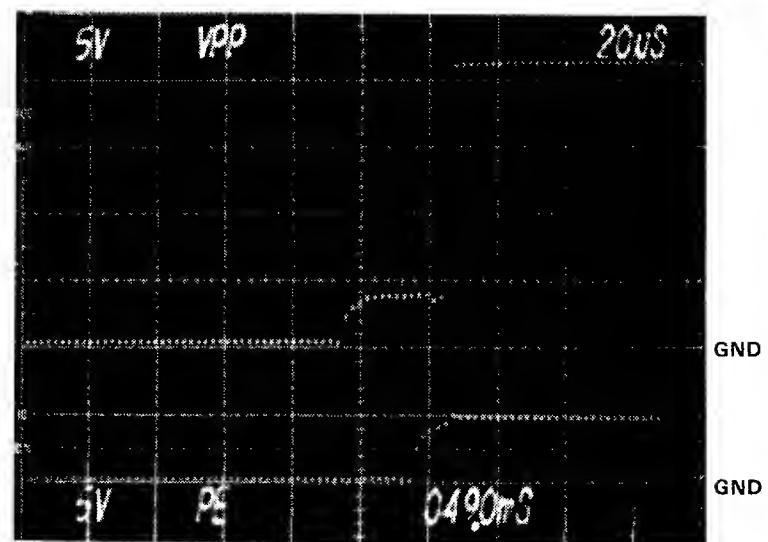
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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.00	6.00	V	
	VPP	20.5	21.0	21.5	V	
	VppV	0.0	0.0	0.8	V	
	tpw	48	50	52	ms	NA NA
	tr	50				
	tf					
	Reject		1		Pulses	
1ST PASS VERIFY	Overprogram		0		Pulses	
	VCC	4.9	5.0	5.1	V	
	VREF	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	VCC	4.9	5.0	5.1	V	
	VREF	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.

## REVISIONS

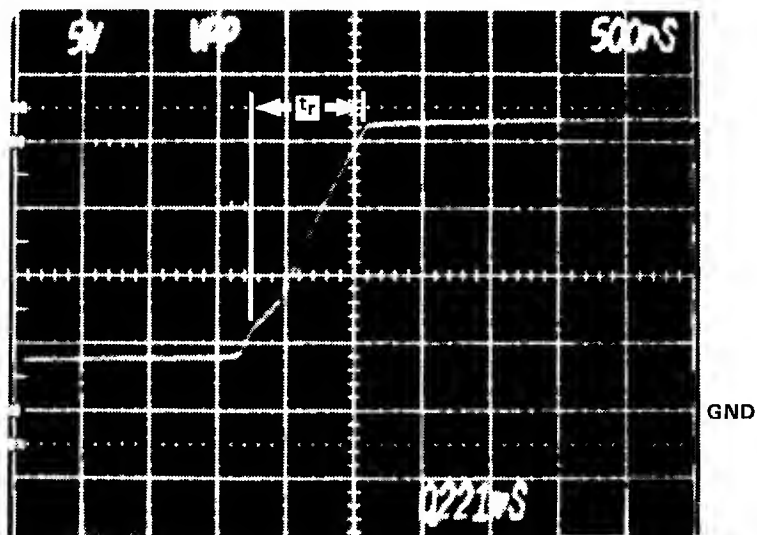
LTR	DESCRIPTION	P. E.	DATE
A	Release	RLS	5/25/83

TIMING DIAGRAM

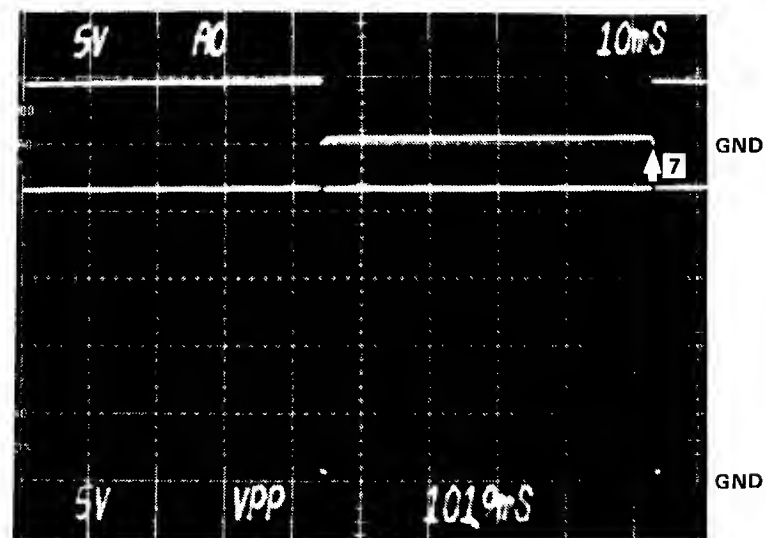
FAMILY CODE 27

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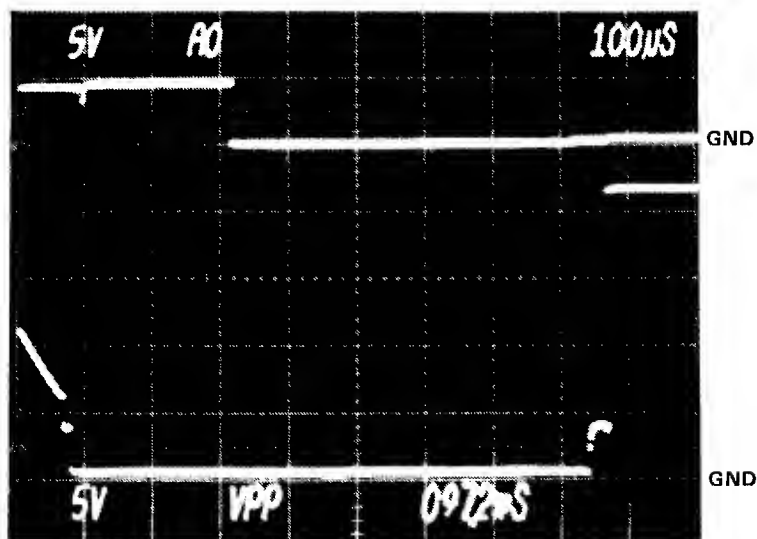
**DATA I/O**



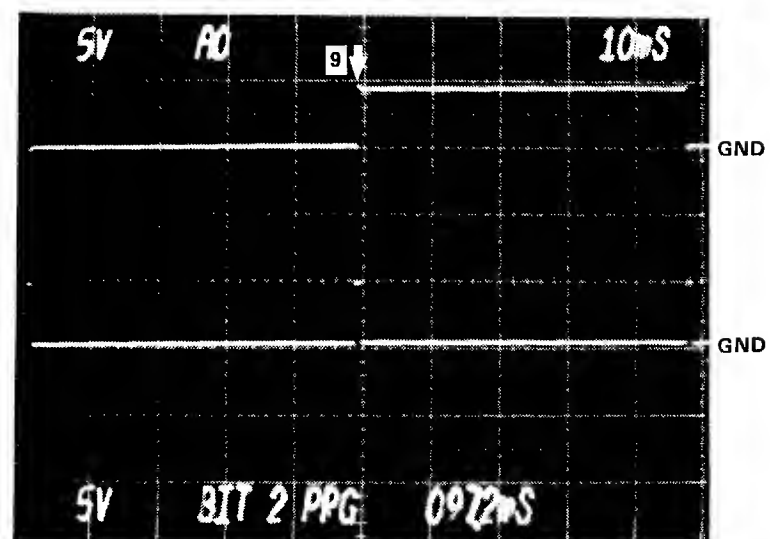
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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

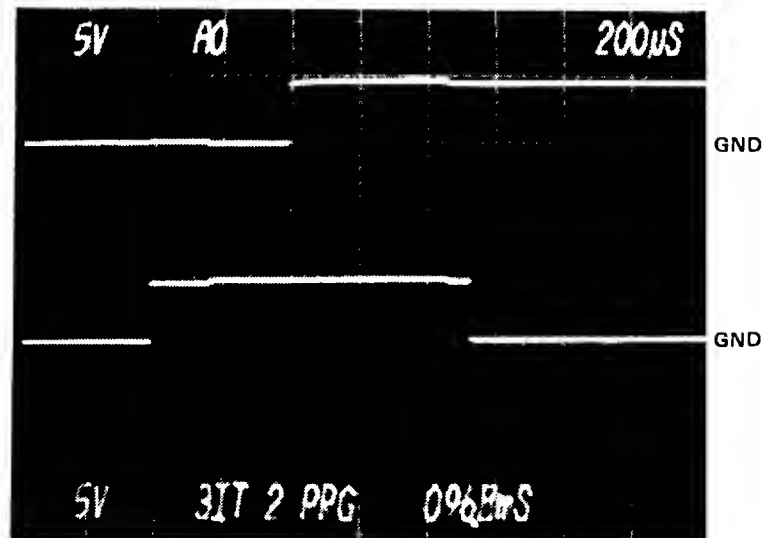
TIMING DIAGRAM

FAMILY CODE 27

Sheet 2 of 3

**DATA I/O**





# REVISIONS

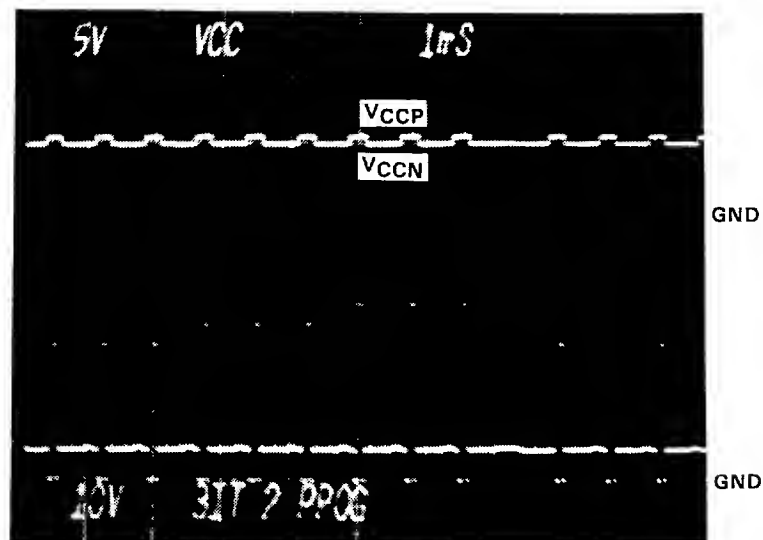
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

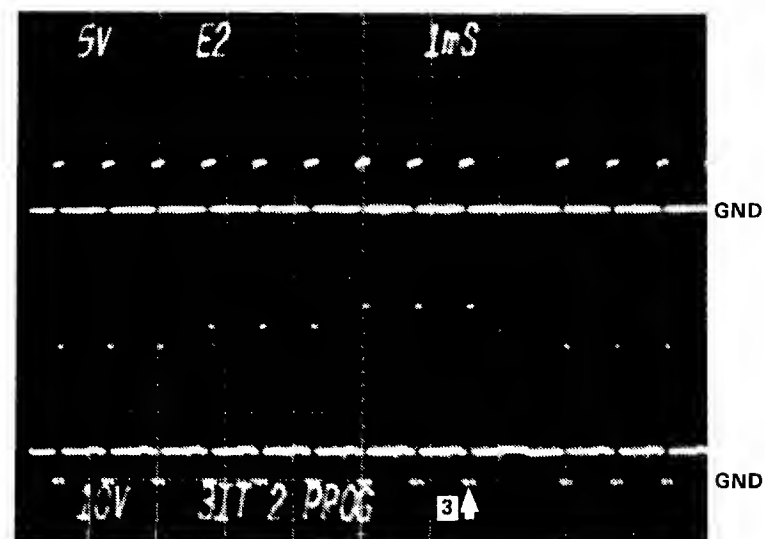
FAMILY CODE 27

Sheet 3 of 3

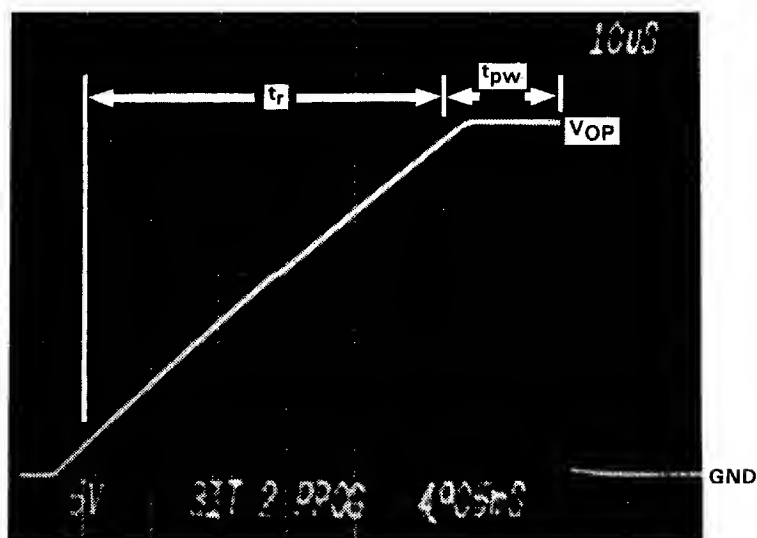
**DATA I/O**



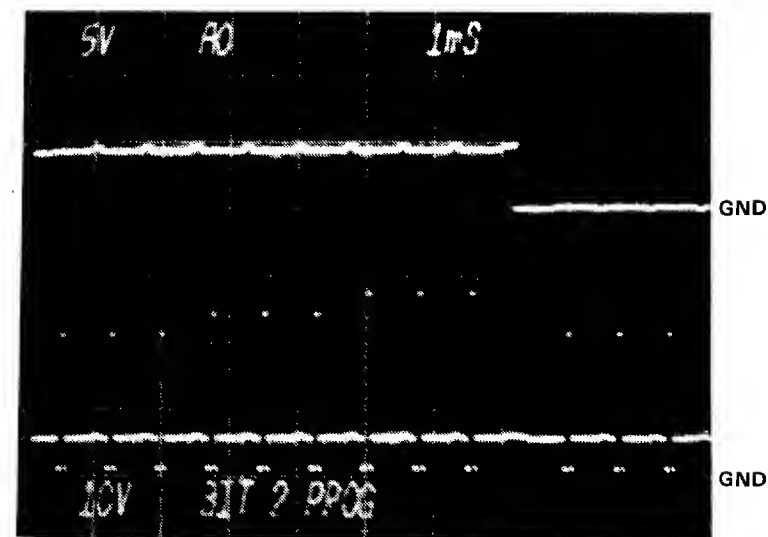
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.4	5.5	5.6	V	
	V <sub>CCN</sub>	4.75	5.0	5.25	V	
	V <sub>OP</sub>	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	t <sub>pw</sub>	10		40	μs	
	t <sub>r</sub>	42	52	69	μs	See note 2
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.1	4.2	4.3	V	
	V <sub>REF</sub>	0.8	0.9	1.0	V	702-1775/TP18
	High Load	13.4	13.7	14.1	V	702-1775/TP15
	Low Load	13.4	13.7	14.1	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	5.9	6.0	6.1	V	
	V <sub>REF</sub>	2.9	3.0	3.1	V	702-1775/TP18
	High Load	0.0	0.0	0.4	V	702-1775/TP15
	Low Load	7.1	7.5	7.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. This is measured from 10% to 90% on the 26V pulses.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	R22	5/25/03

**TIMING DIAGRAM**

**FAMILY CODE 29**

Sheet 1 of 1 **DATA I/O**



## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	NA
	V <sub>OP</sub>					
	V <sub>PP</sub>	24.0	25.0	26.0	V	
	V <sub>PPV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	4.9	5.0	5.1	ms	
	t <sub>r</sub>	5			ns	See note 2
	t <sub>f</sub>	5			ns	
	Reject		5		Pulses	
	Overprogram		x		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. The number of overprogram pulses is equal to the greatest number of reject pulses applied to any address.

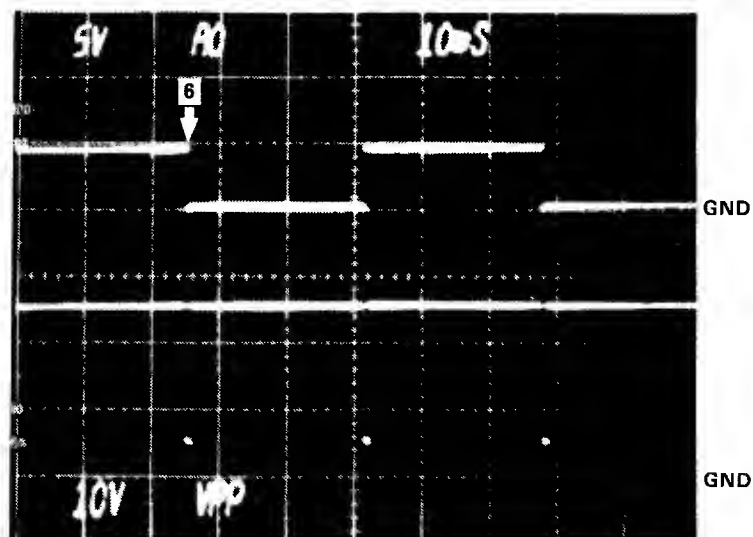
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	R22	5/25/03

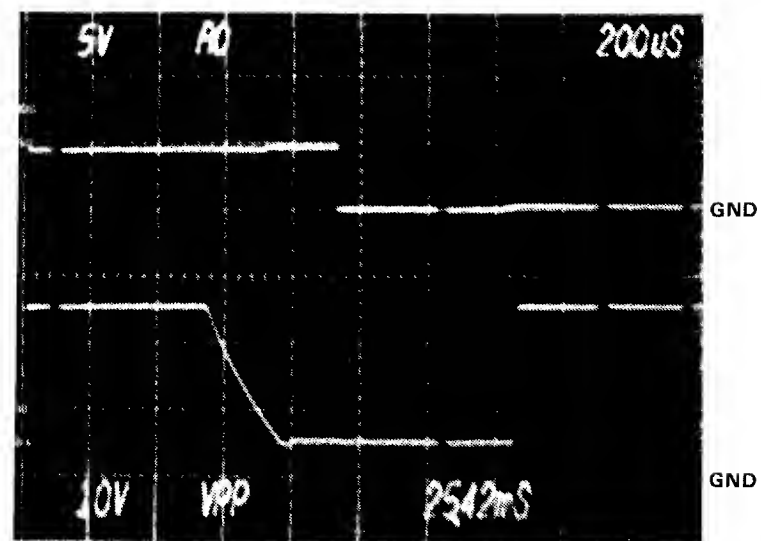
TIMING DIAGRAM

FAMILY CODE 31

Sheet 1 of 2 **DATA I/O**



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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

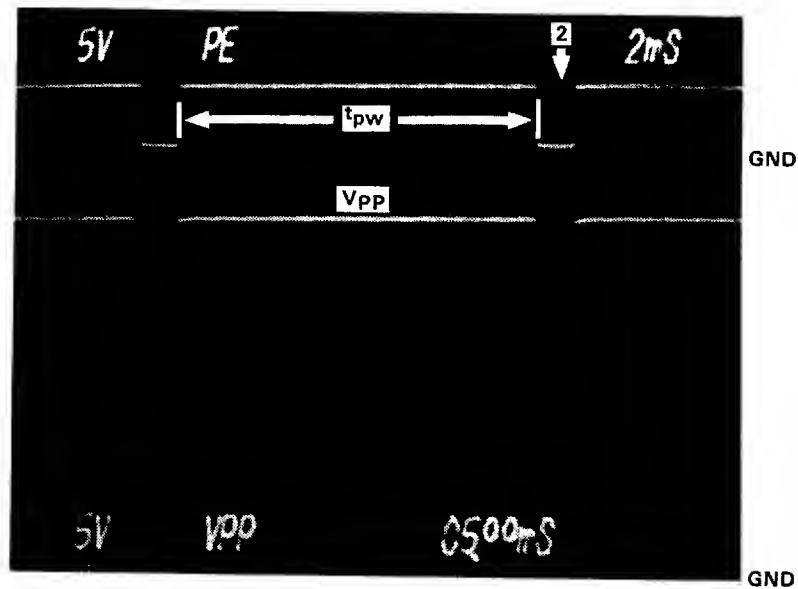
TIMING DIAGRAM

FAMILY CODE 31

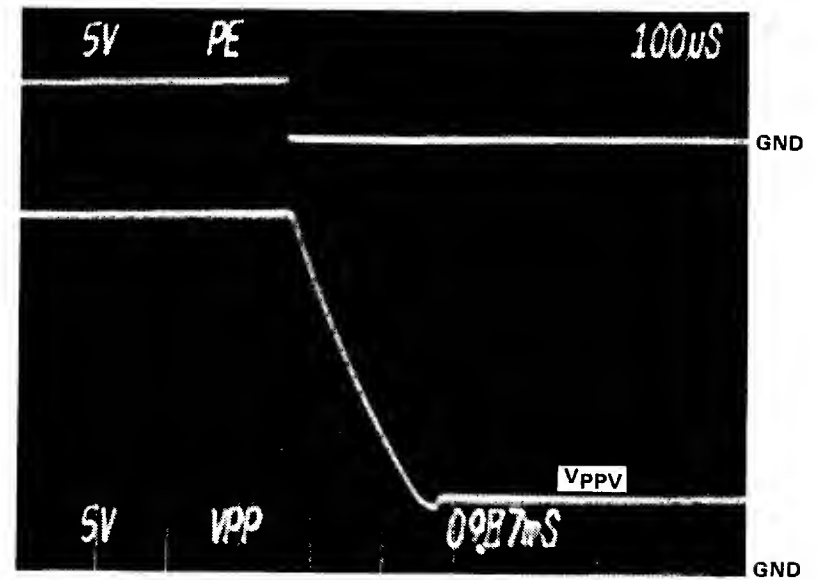
Sheet 2 of 2

**DATA I/O**

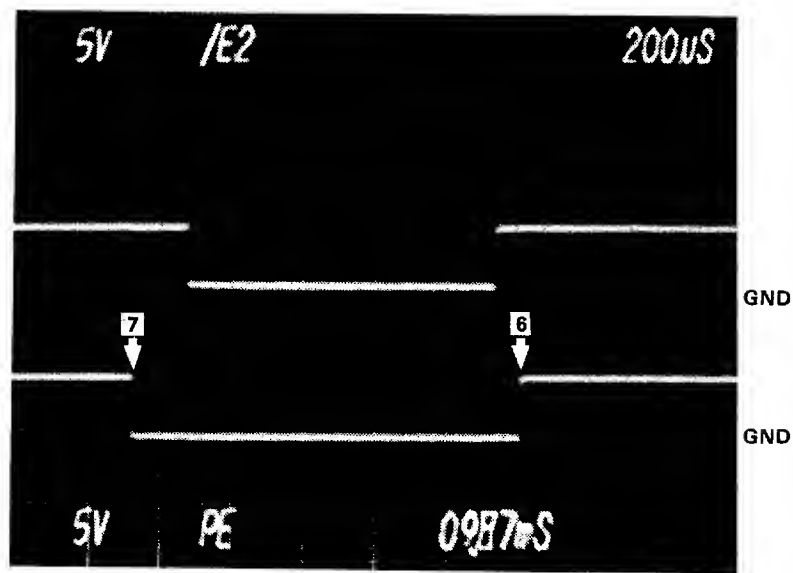




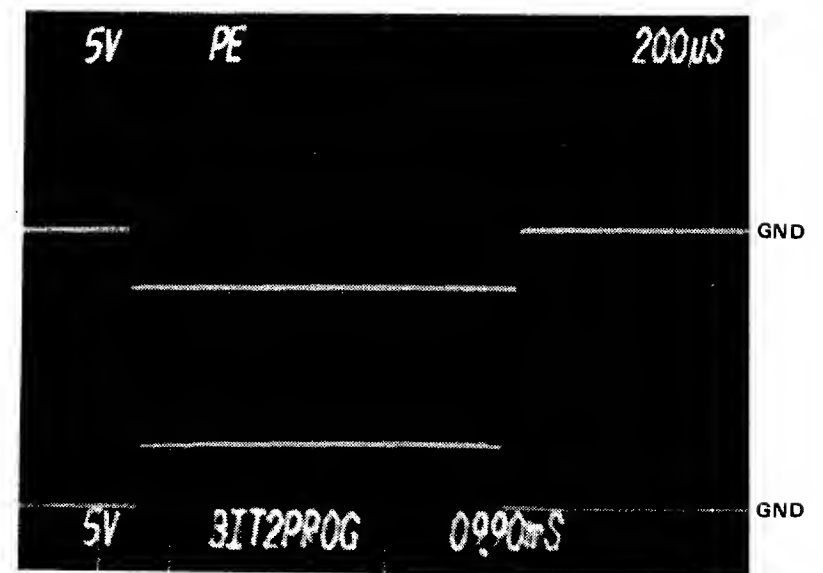
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	24.0	25.0	26.0	V	
	V <sub>PPV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	15	20	25	ms	See note 2
	t <sub>r</sub>	5			ns	
	t <sub>aw</sub>	19.0	20.0	21.0	ms	Not Shown
	t <sub>f</sub>	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. Photos show t<sub>pw</sub> = 10ms, actual waveform should conform to table.

## REVISIONS

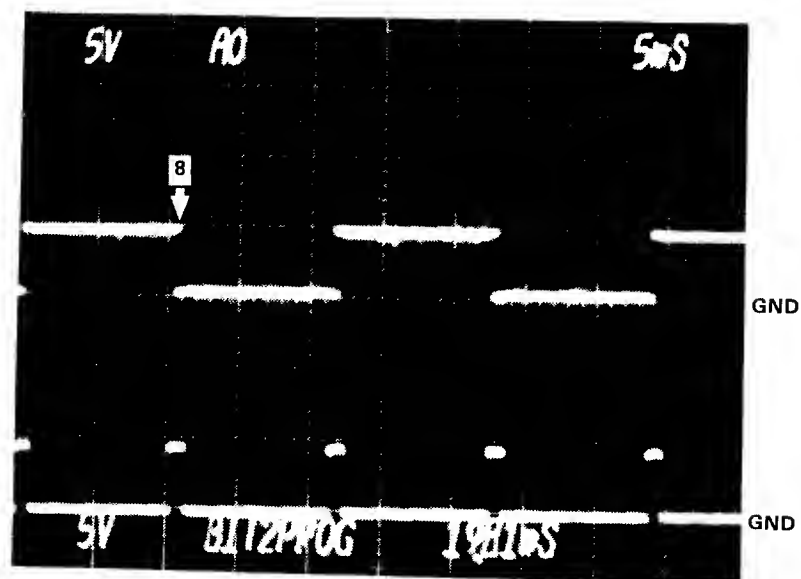
LTR	DESCRIPTION	P.E.	DATE
A	Release	RSS	5/25/83

TIMING DIAGRAM

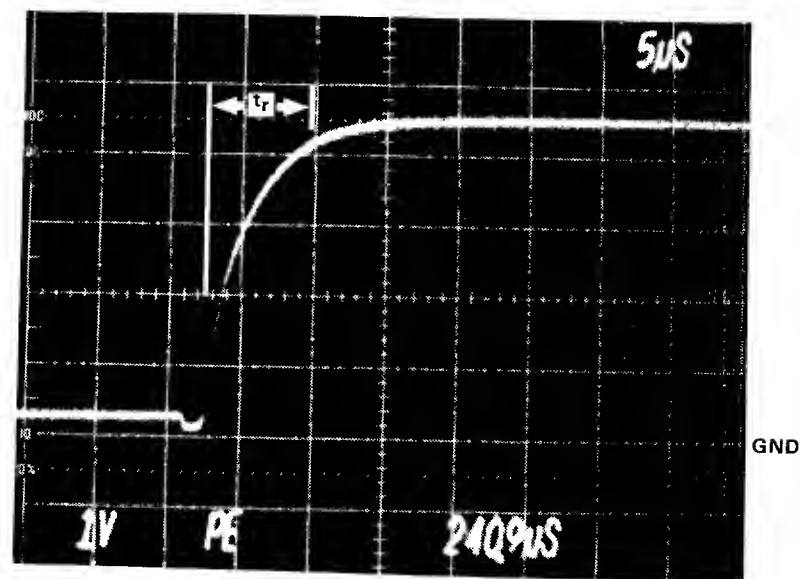
FAMILY CODE 33

Sheet 1 of 2

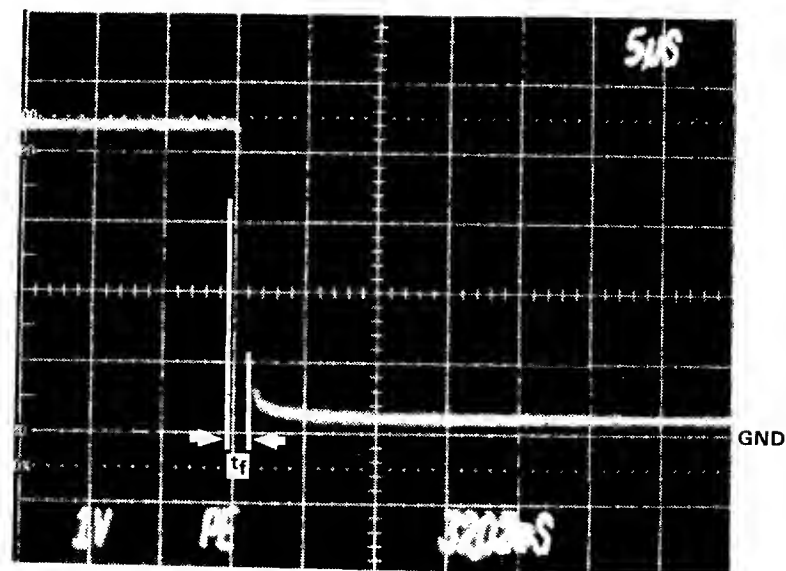
# DATA I/O



5



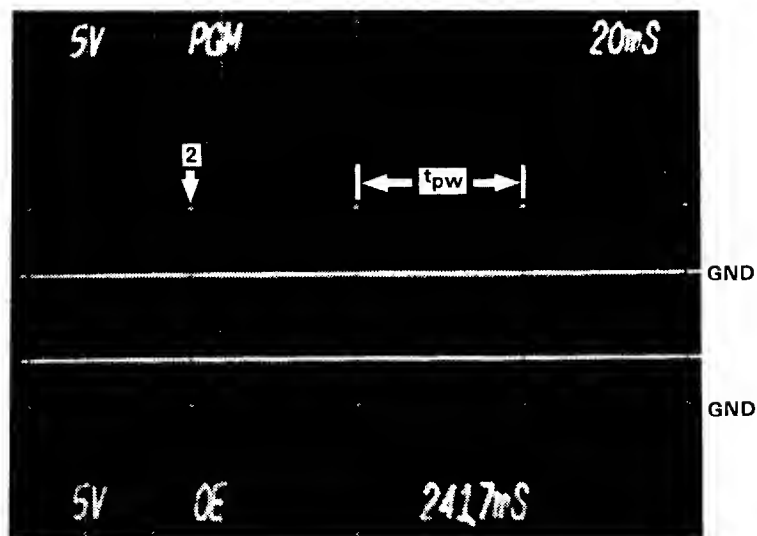
6



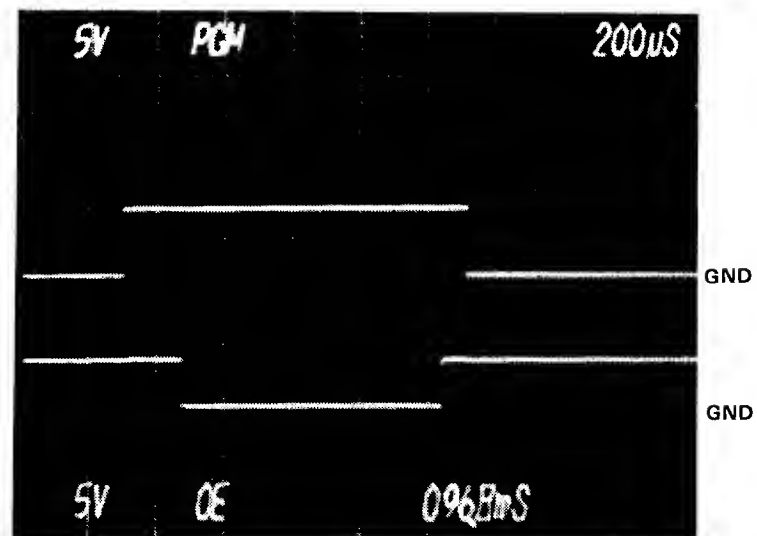
7

# REVISIONS

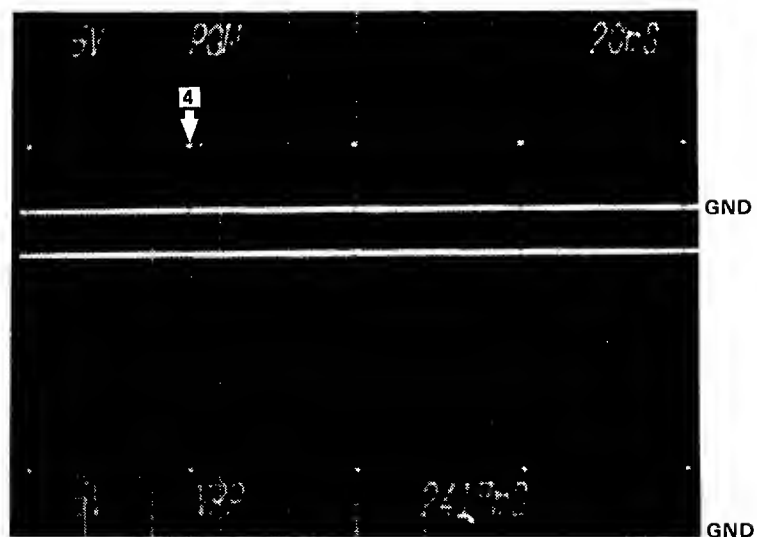
LTR	DESCRIPTION	P.E.	DATE	<p>TIMING DIAGRAM</p> <p>FAMILY CODE 33</p> <p>Sheet 2 of 2 <b>DATA I/O</b></p>
	See Sheet 1			



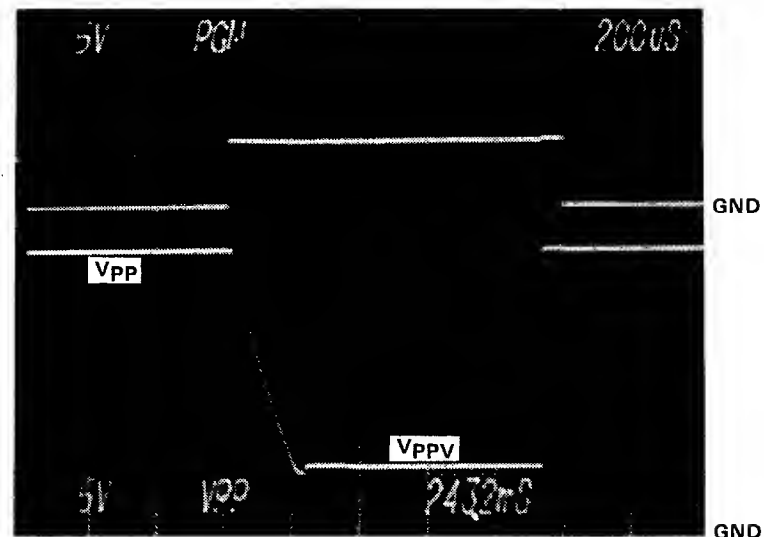
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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.0	5.1	5.3	V	NA
	V <sub>pp</sub>					
	V <sub>OP</sub>	27.3	27.8	28.3	V	Saa nota 4
	t <sub>pw</sub>	7.0	7.5	8.0	µs	
	t <sub>r</sub>	0.21		0.5	µs	
	t <sub>f</sub>	0.3		0.8	µs	
	Overprogram		4		Pulsas	See note 5
	Reject		1000		Pulses	
	Duty Cycle	20	23	26	%	
1ST PASS	V <sub>CC</sub>	4.0	4.1	4.2	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
VERIFY	V <sub>REF</sub>	.7	.8	.9	V	
	High Load	17.5	18.0	18.5	V	
	Low Load	17.5	18.0	18.5	V	
2ND PASS	V <sub>CC</sub>	6.4	6.5	6.6	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
VERIFY	V <sub>REF</sub>	3.9	4.0	4.1	V	
	High Loed		0.0	0.5	V	
	Low Loed	5.4	5.7	6.0	V	

## NOTES

1. Load RAM with \$01.
2. Use a 150Ω Id. on BTP for all waveforms except photo #3. Photo #3 should have no Id. on BTP.
3. Do not use a wirewound Id. resistor.
4. Measurement taken at 15V point of 01 with a 150Ω Id.
5. 1000 pulses equals 30 ms as shown in photo #3.

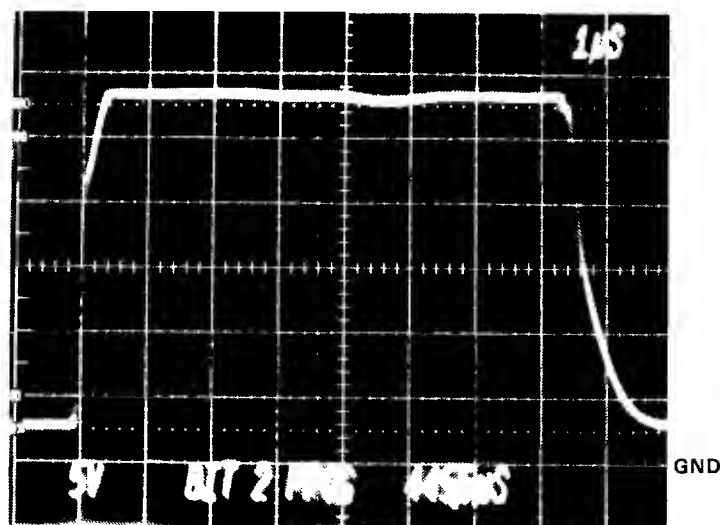
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RLL	5/25/83

TIMING DIAGRAM

FAMILY CODE 72

Sheet 1 of 2 **DATA I/O**



## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown
	V <sub>OP</sub>	3.8	5.0	6.0	V	
	V <sub>PP</sub>	20.5	21.0	21.5	V	
	V <sub>PPV</sub>	4.75	5.00	5.25	V	
	t <sub>pw</sub>	48	50	52	ms	
	t <sub>r</sub>					
	t <sub>f</sub>					
	Reject		1		Pulses	
1ST PASS VERIFY	Overprogram		0		Pulses	NA NA  702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	
	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
2ND PASS VERIFY	Low Load	13.1	13.5	13.9	V	

## NOTES

1. Load RAM with \$FE.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RLS	5/25/03

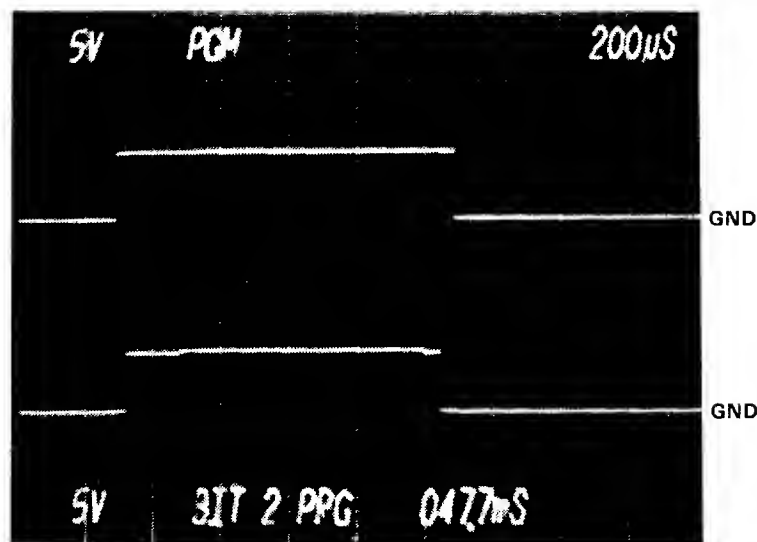
**TIMING DIAGRAM**

**FAMILY CODE 35**

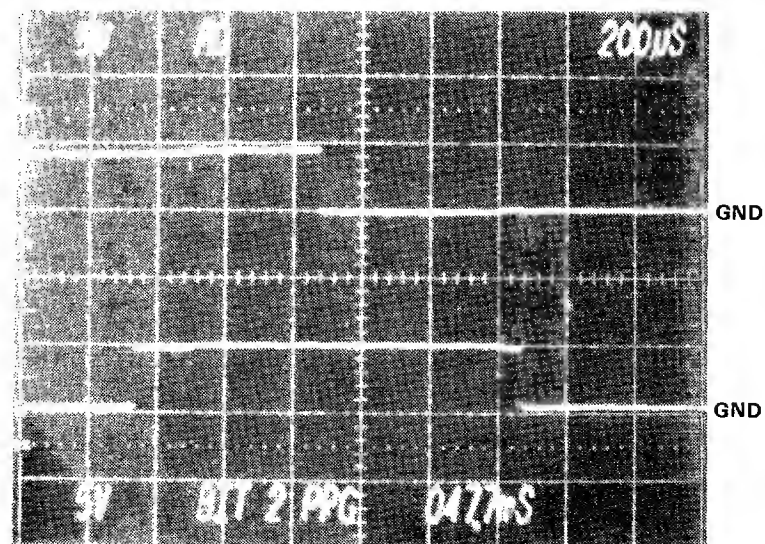
Sheet 1 of 2

# DATA I/O

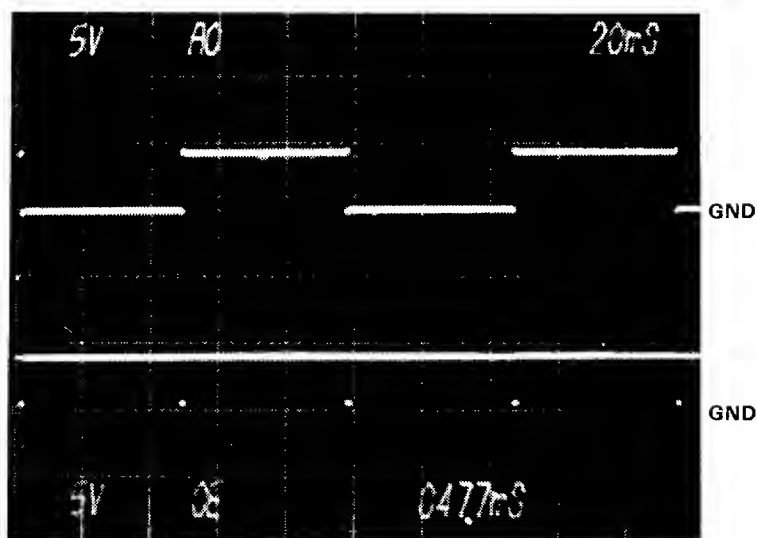




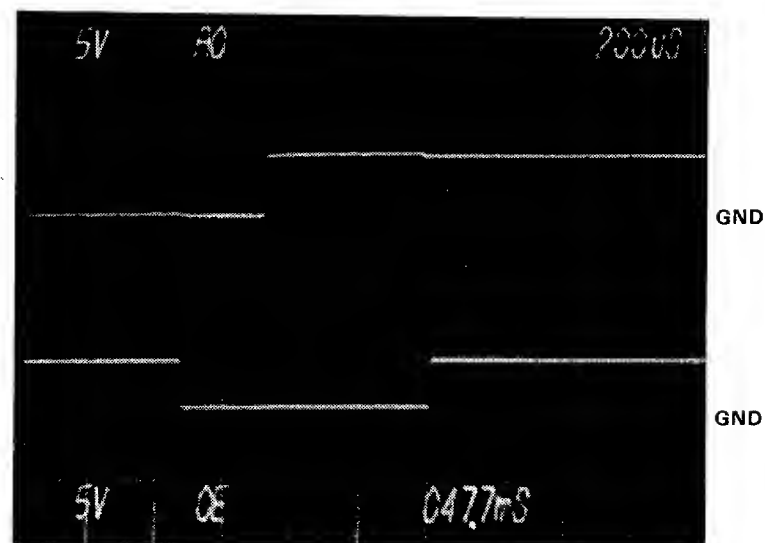
5



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# REVISIONS

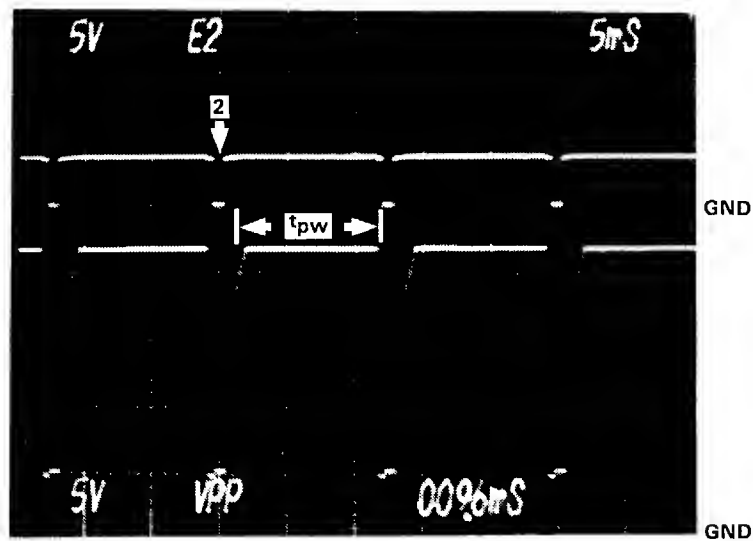
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

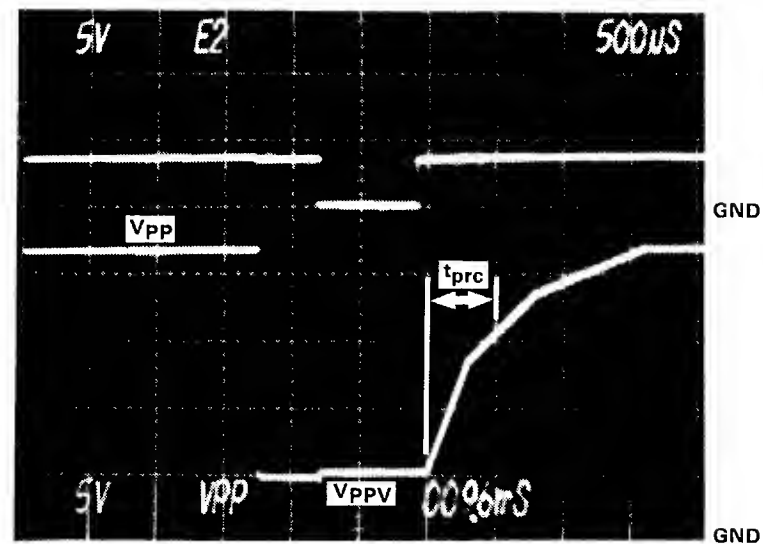
FAMILY CODE 35

Sheet 2 of 2

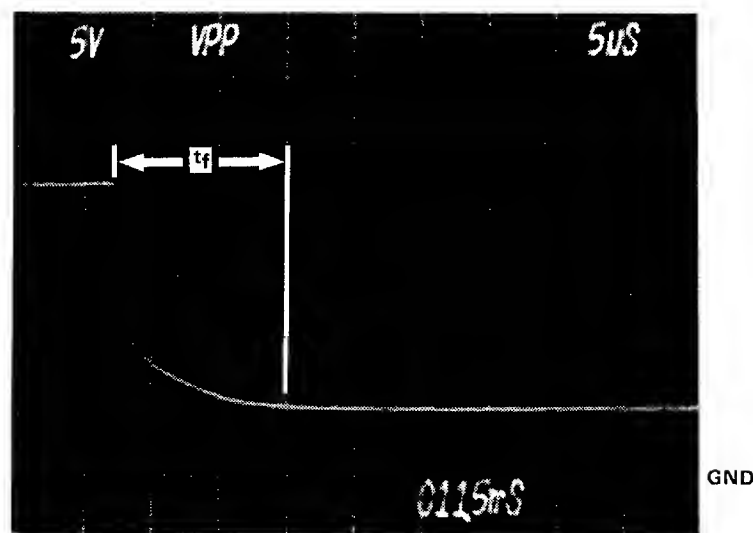
**DATA I/O**



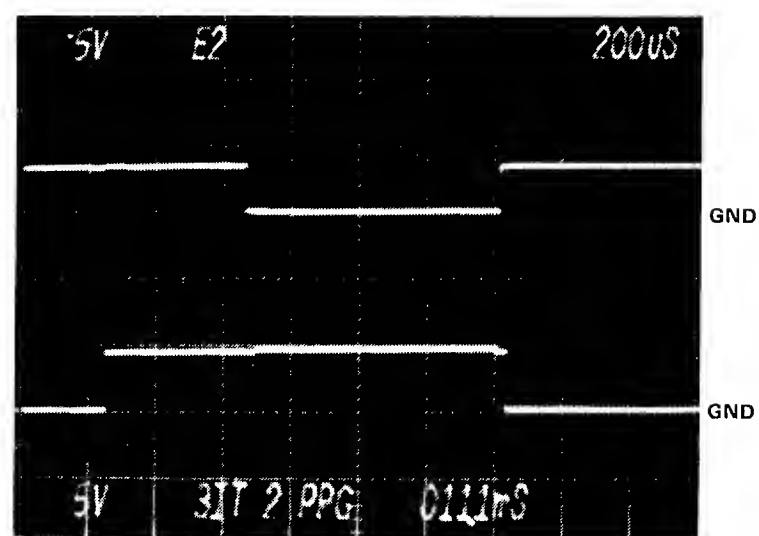
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown NA
	V <sub>OP</sub>					
	V <sub>PP</sub>	20.0	21.0	22.0	V	
	V <sub>PPV</sub>	4.0	5.0	6.0	V	
	V <sub>OE</sub>	9.0	12.0	15.0	V	
	t <sub>pw</sub>	9.0	10.0	15.0	ms	See note 2
	t <sub>prc</sub>	450	600	750	μs	
	t <sub>f</sub>			100	μs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	0.4	0.5	0.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	2.3	2.4	2.5	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. TPRC is measured from 6v to 15.5v.
3. Erase waveforms same as photos 1 and 2.

## REVISIONS

LTR	DESCRIPTION	P. E.	DATE
A	Release	R88	5/25/83

**TIMING DIAGRAM**

**FAMILY CODE 37**

Sheet 1 of 2

# DATA I/O



# REVISIONS

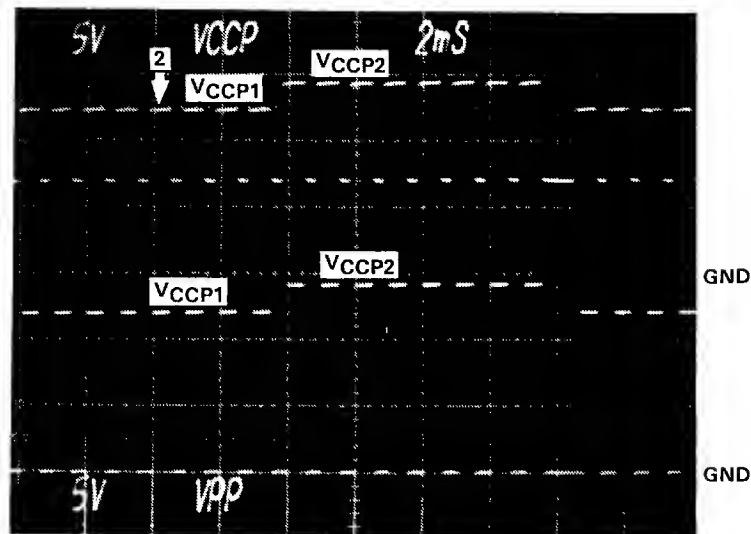
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

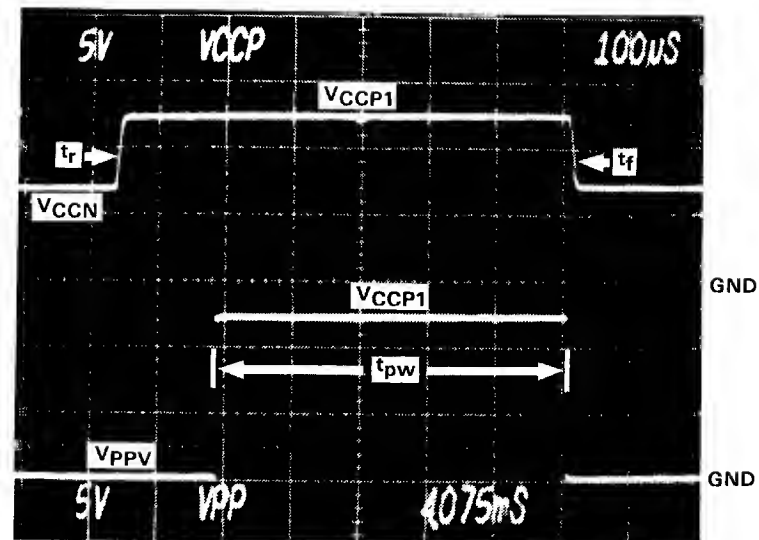
FAMILY CODE 37

Sheet 2 of 2

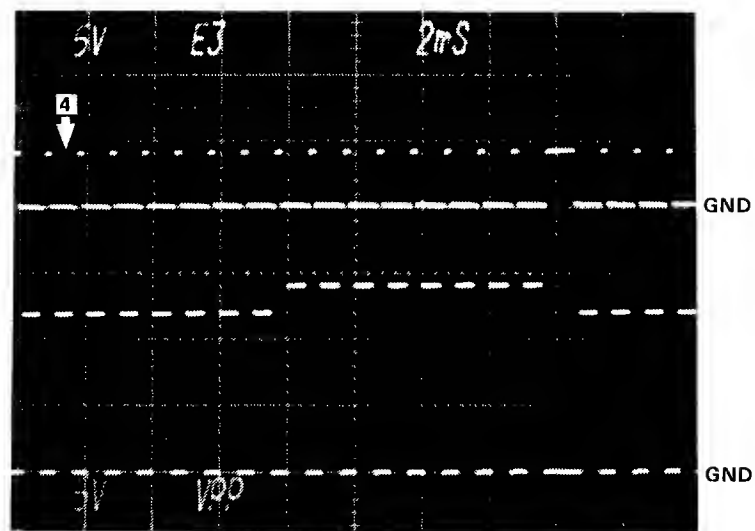
**DATA I/O**



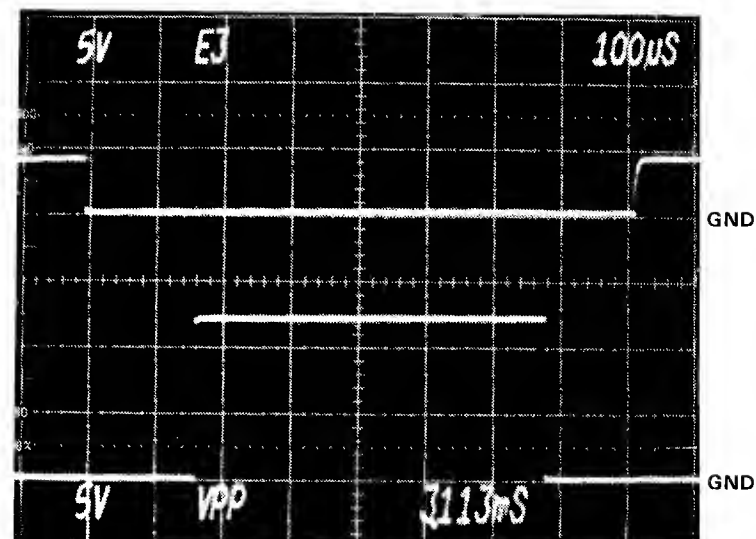
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCN	6.0	6.5	7.0	V	
	VCCP1	11.5	12.0	12.5	V	Pulses 1-8
	VCCP2	13.5	14.0	14.5	V	Pulses 9-16
	VPP1	11.5	12.0	12.5	V	Pulses 1-8
	VPP2	13.5	14.0	14.5	V	Pulses 9-16
	VPPV	0.0		1.0	V	
	VOP1	11.5	12.0	12.5	V	Pulses 1-8
	VOP2	13.5	14.0	14.5	V	Pulses 9-16
	t <sub>pw</sub>	450	500	550	μs	
	t <sub>r</sub>	1.0			μs	
	t <sub>f</sub>	1.0			μs	
	Reject		16		Pulses	
1ST PASS VERIFY	Overprogram		2		Pulses	
	V <sub>CC</sub>	3.9	4.0	4.1	V	
	V <sub>REF</sub>	0.7	0.8	0.9	V	702-1775/TP18
	High Load	4.5	4.9	5.3	V	702-1775/TP15
2ND PASS VERIFY	Low Load	4.5	4.9	5.3	V	702-1775/TP14
	V <sub>CC</sub>	5.9	6.0	6.1	V	
	V <sub>REF</sub>	4.0	4.1	4.2	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	7.1	7.5	7.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$01.
2. V<sub>CC</sub> is loaded with 100Ω, 2 watt resistor.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	REG	5/25/83

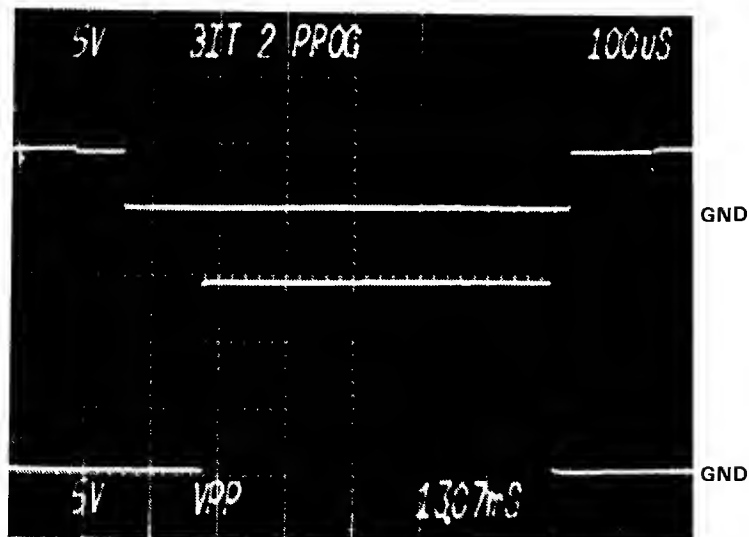
TIMING DIAGRAM

FAMILY CODE 40

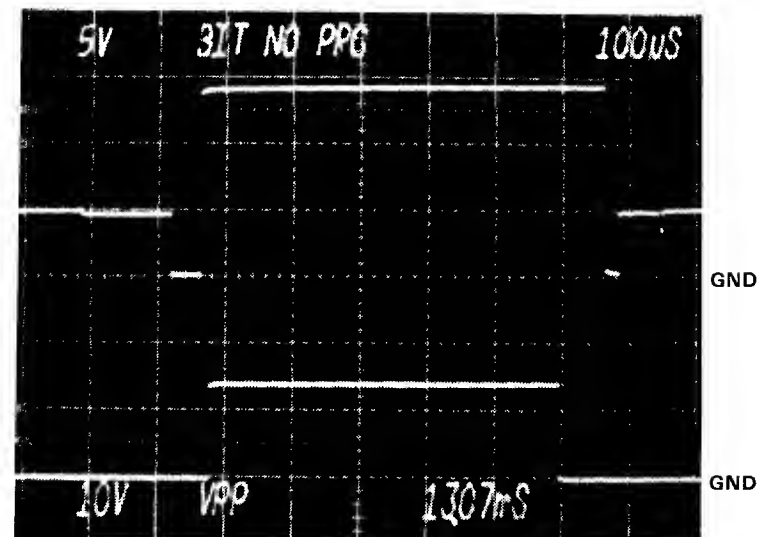
Sheet 1 of 2

# DATA I/O

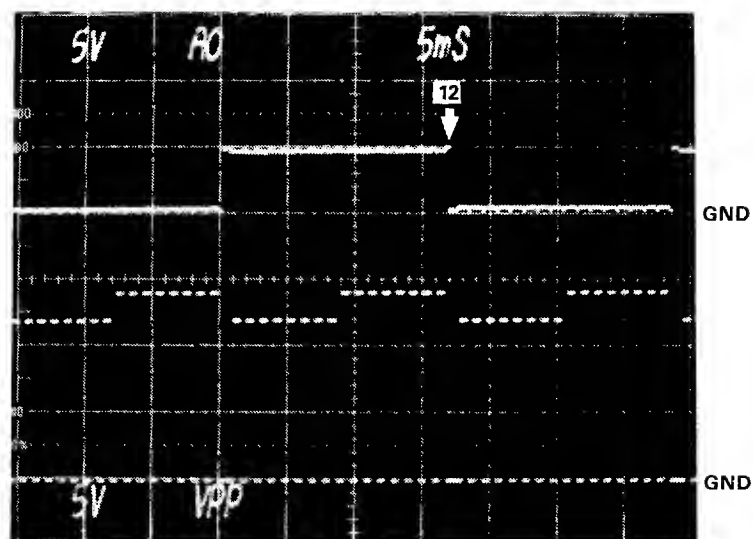




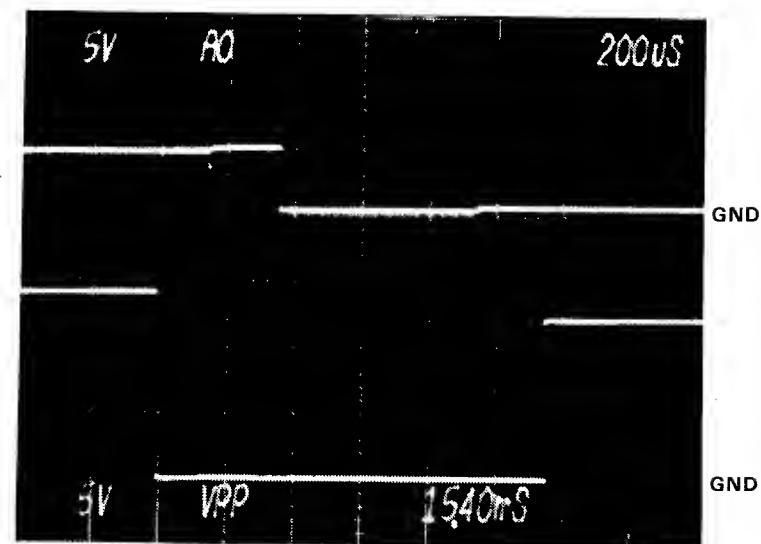
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# REVISIONS

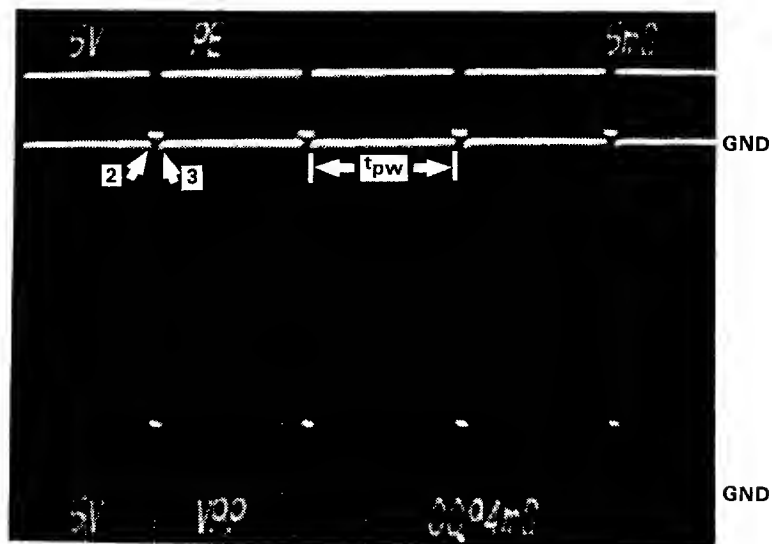
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

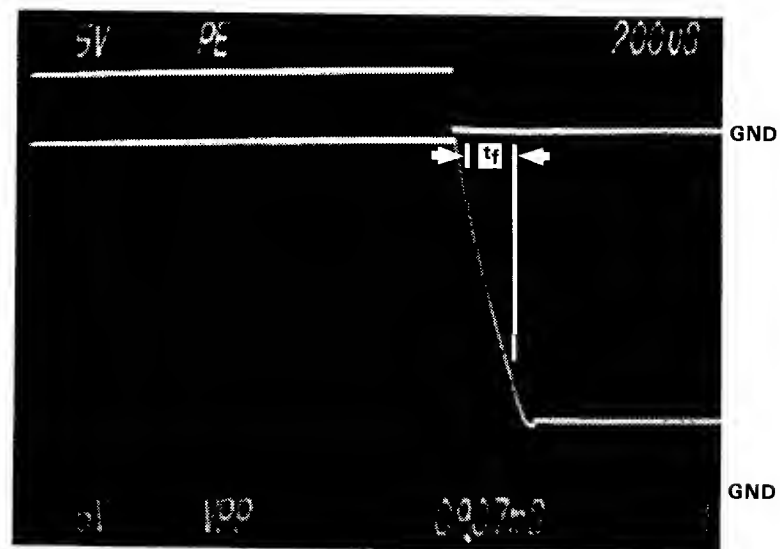
FAMILY CODE 40

Sheet 2 of 2

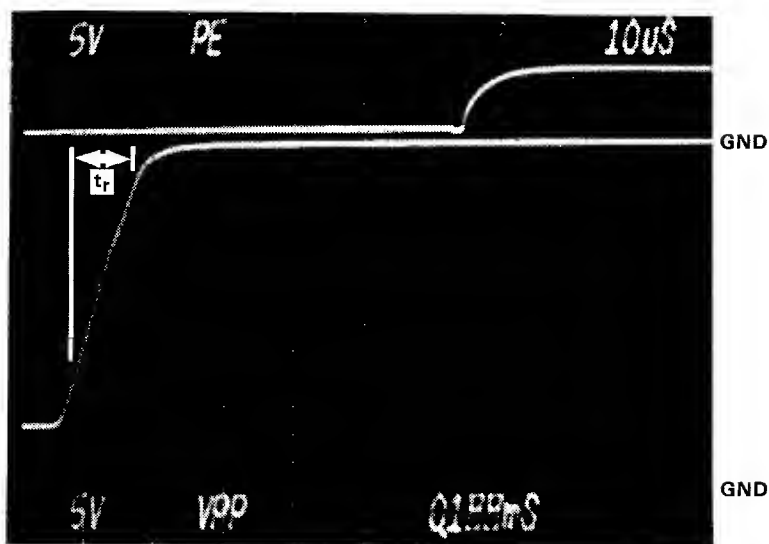
**DATA I/O**



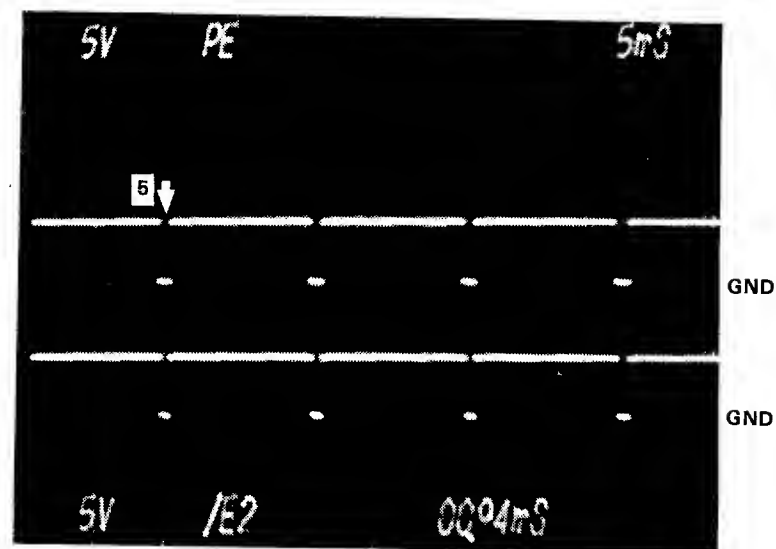
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown NA
	V <sub>OP</sub>					
	V <sub>PP</sub>	24.0	25.0	26.0	V	
	V <sub>PPV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	9.8	10.0	10.2	ms	
	t <sub>r</sub>	50			ns	
	t <sub>ep</sub>	96	100	102	ms	
	t <sub>f</sub>	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	

## NOTES

1. Load RAM with \$FE.
2. Photo 10 is the erase waveform.

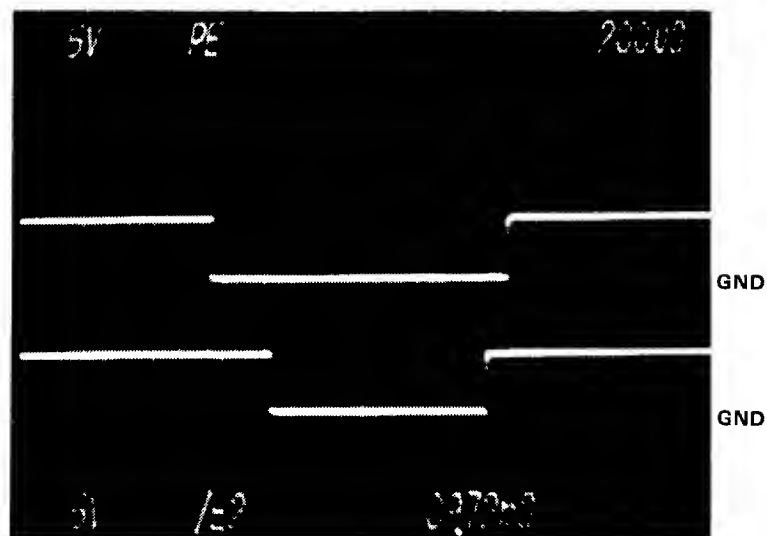
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	<i>RJS</i>	<i>5/25/83</i>

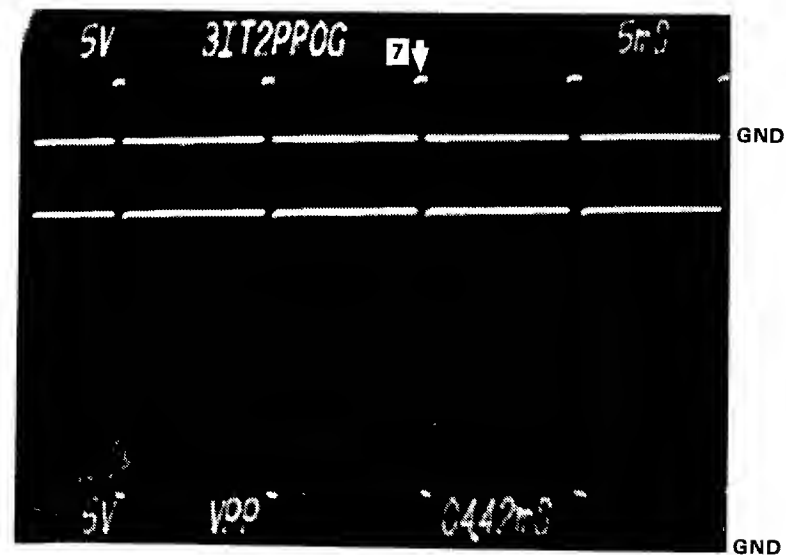
TIMING DIAGRAM

FAMILY CODE 43

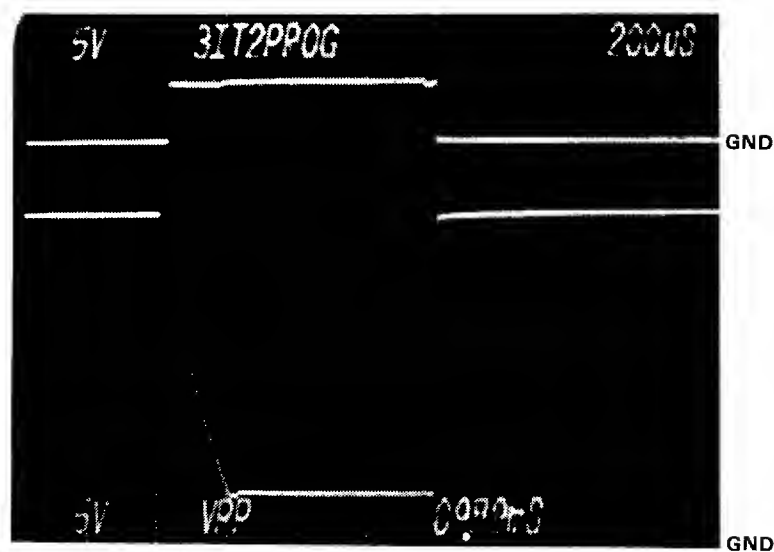
Sheet 1 of 3 **DATA I/O**



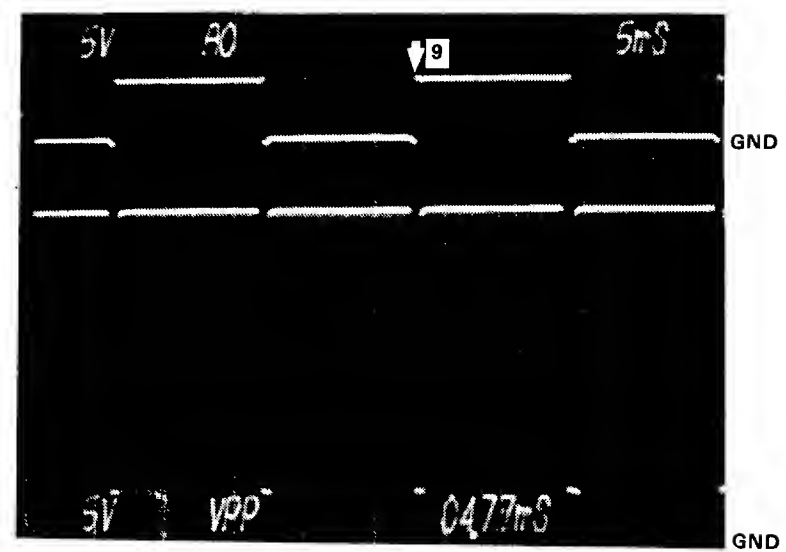
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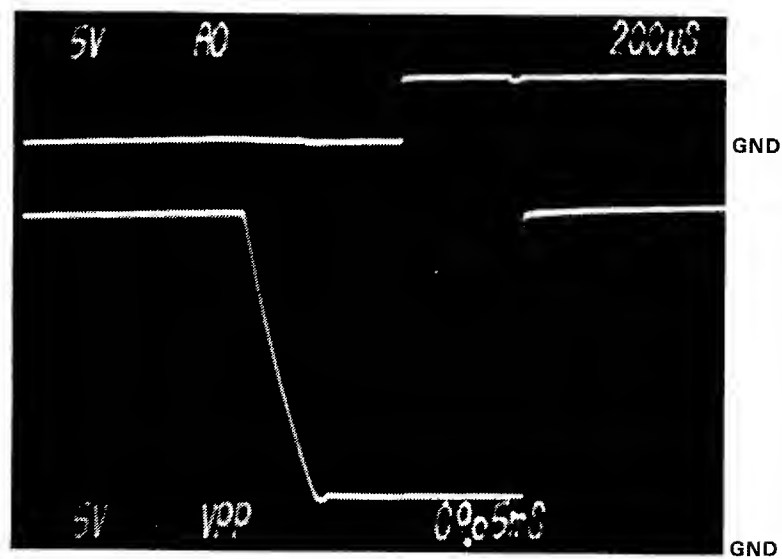
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

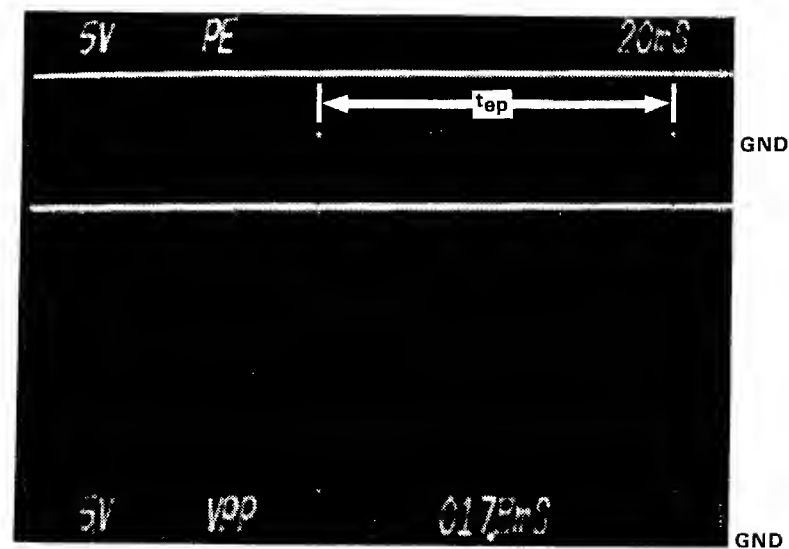
TIMING DIAGRAM

FAMILY CODE 43

Sheet 2 of 3 **DATA I/O**



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REVISIONS

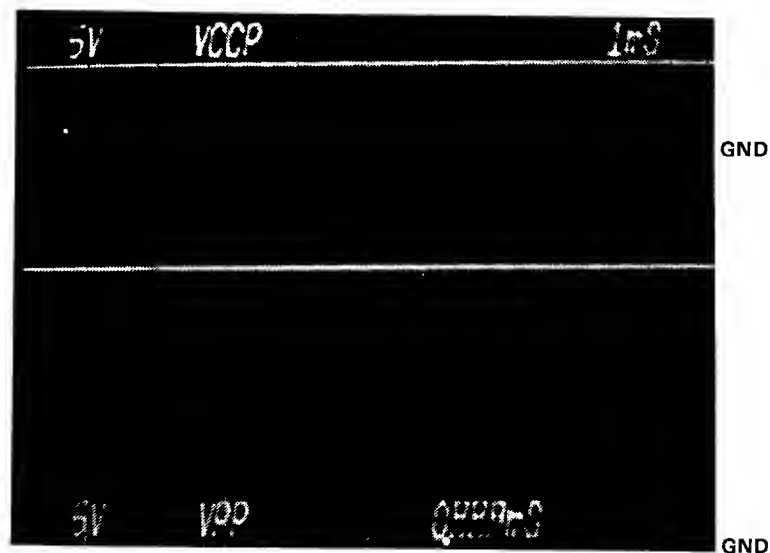
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

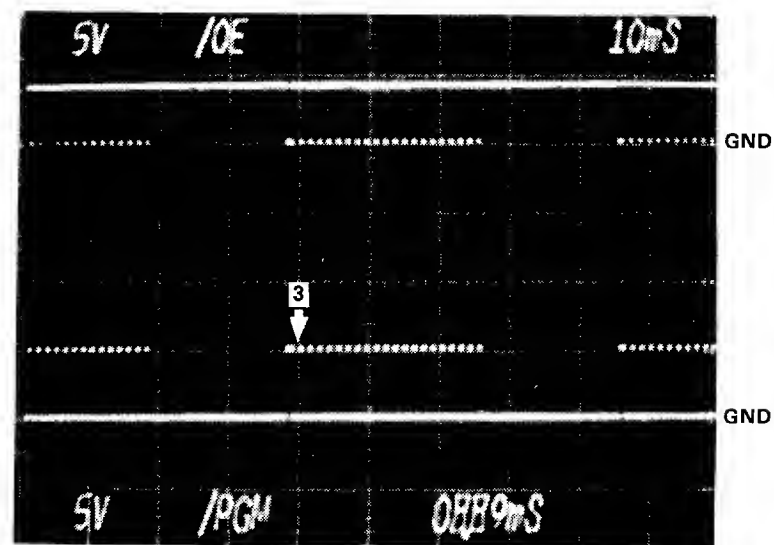
FAMILY CODE 43

Sheet 3 of 3 **DATA I/O**

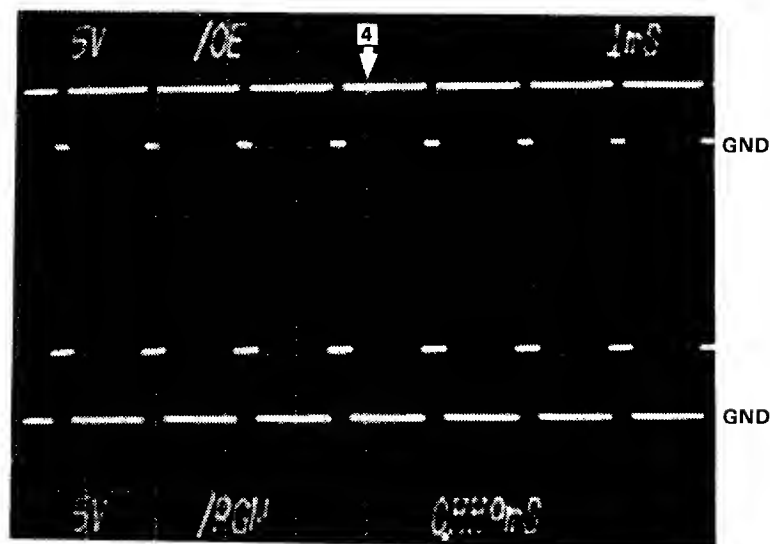




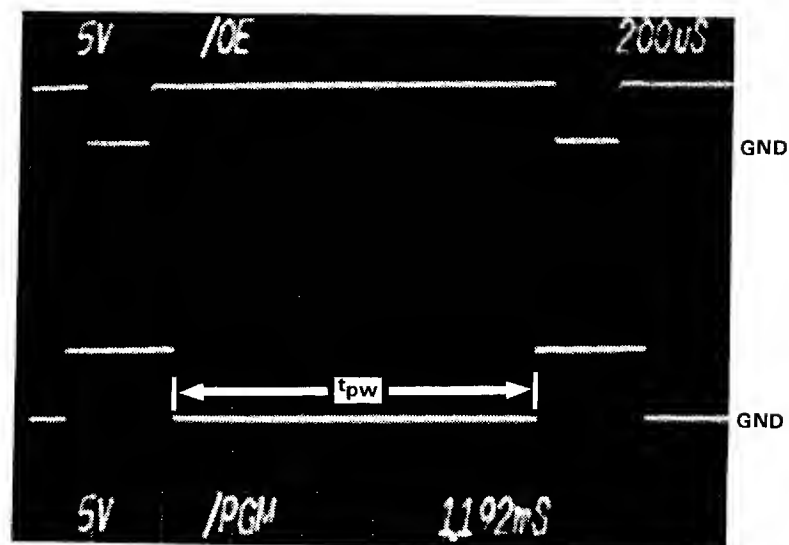
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.75	6.00	6.25	V	
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	20.5	21.0	21.5	V	
	V <sub>PPV</sub>					NA
	t <sub>pw</sub>	.95	1.0	1.05	ms	
	t <sub>r</sub>					NA
	t <sub>f</sub>					NA
	Reject		20		Pulses	
	Overprogram		1		Pulses	See note 2
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>				V	NA
VERIFY	V <sub>REF</sub>				V	NA
	High Load				V	NA
	Low Load				V	NA

## NOTES

1. Load RAM with \$FE.
2. The overprogram pulse follows the reject pulses and it's length is the number of reject pulses multiplied by 1 ms.

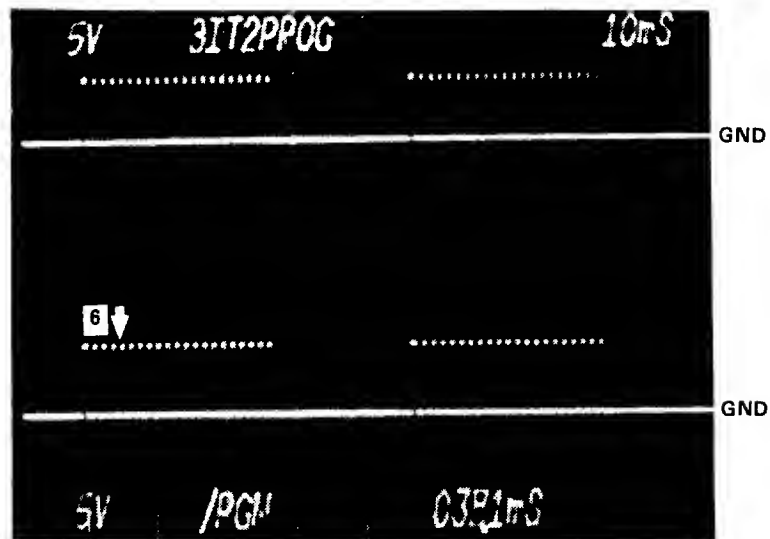
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	R22	5/25/03

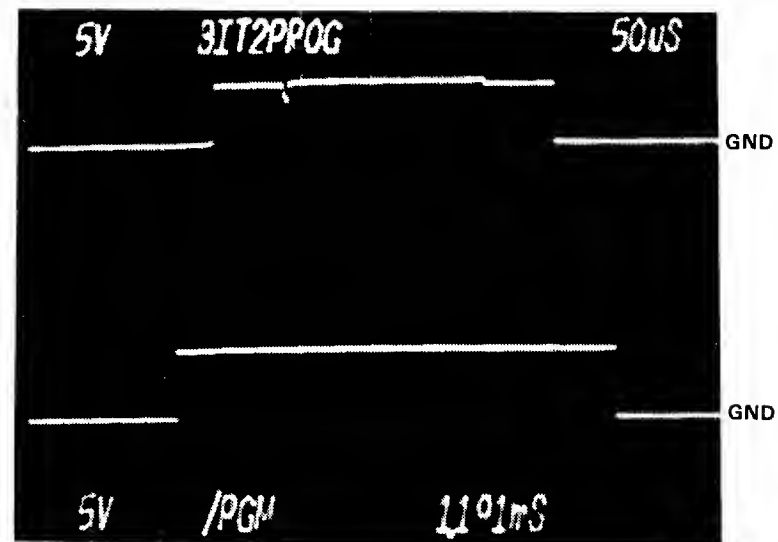
TIMING DIAGRAM

FAMILY CODE 45

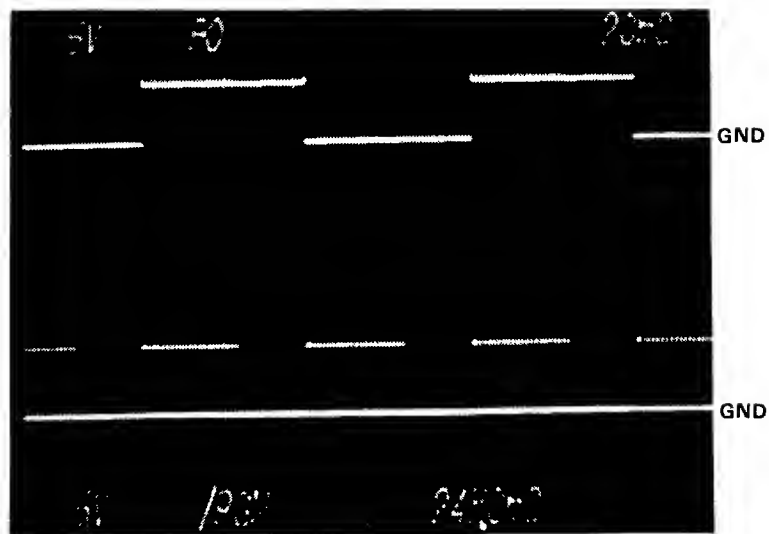
Sheet 1 of 2 **DATA I/O**



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# REVISIONS

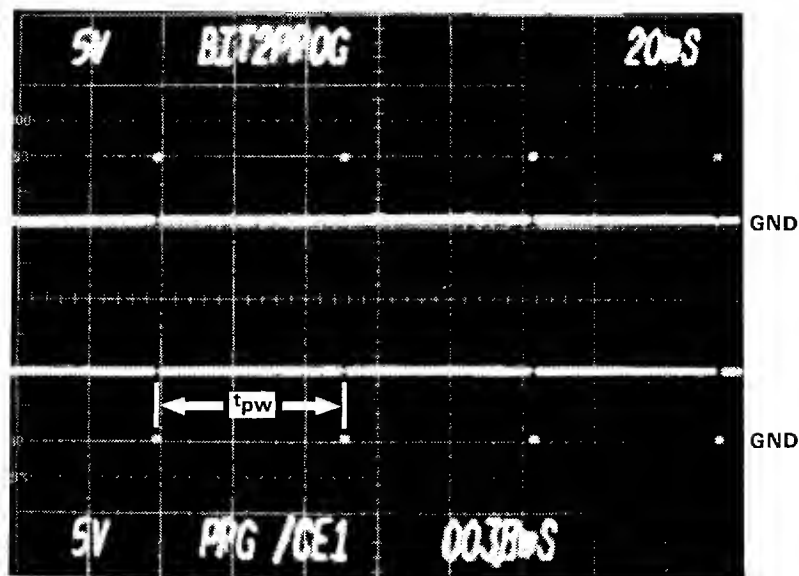
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

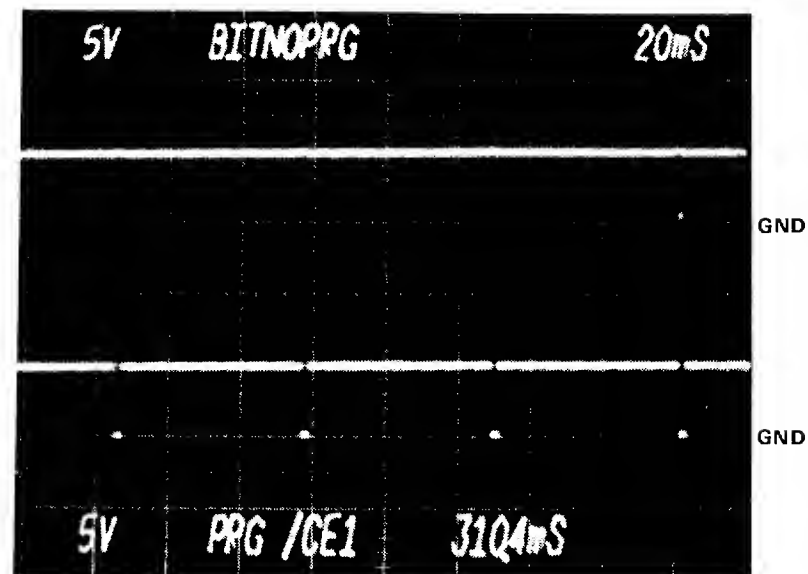
FAMILY CODE 45

Sheet 2 of 2

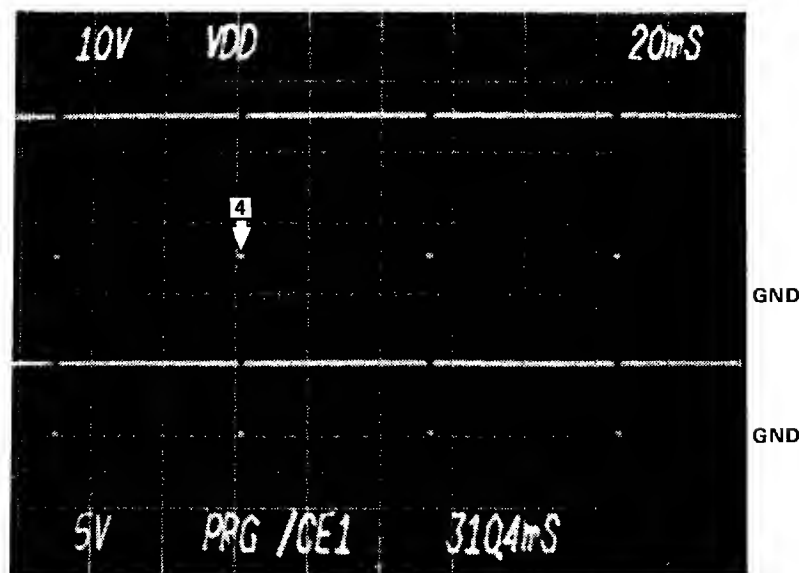
**DATA I/O**



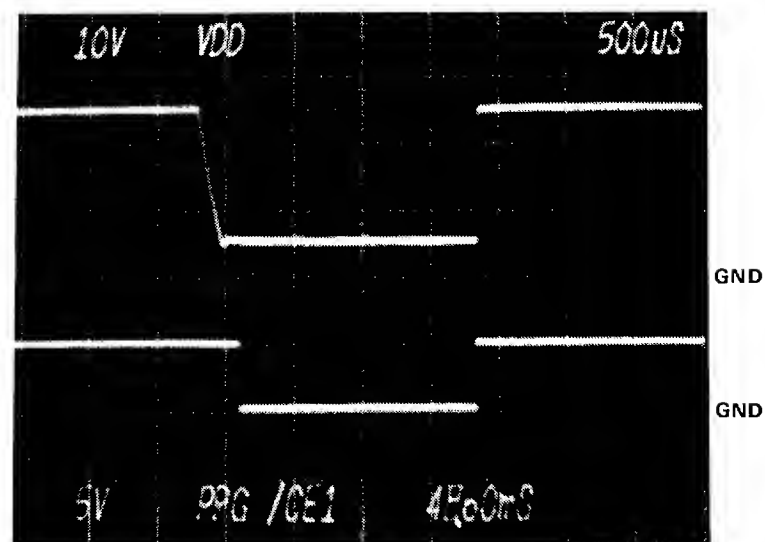
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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	4.25	V	
	V <sub>DDV</sub>	4.75	5.00	5.25		
	V <sub>DDP</sub>	24.0	25.0	26.0	V	
	t <sub>pw</sub>	45	50	55	ms	
	t <sub>r</sub>	.01			μs	
	t <sub>f</sub>	.01			μs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>				V	NA
VERIFY	V <sub>REF</sub>				V	NA
	High Load				V	NA
	Low Load				V	NA

## NOTES

1. Load RAM with \$FE.

## REVISIONS

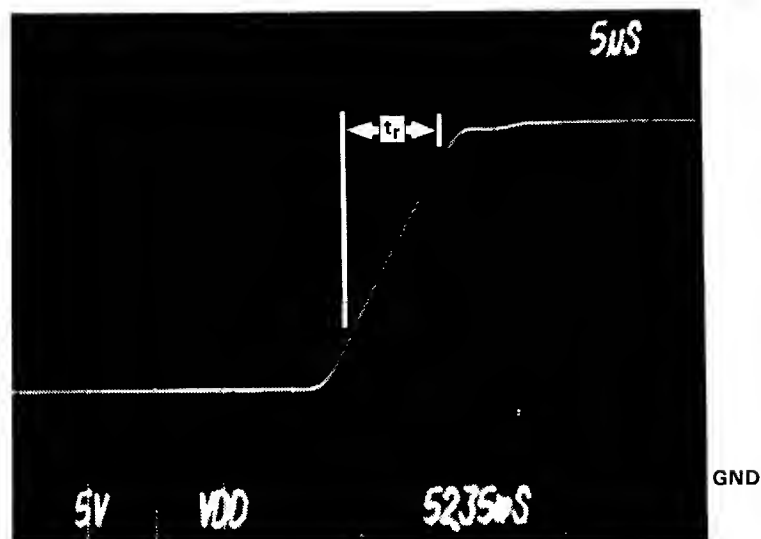
LTR	DESCRIPTION	P.E.	DATE
A	Release	R83	5/25/83

TIMING DIAGRAM

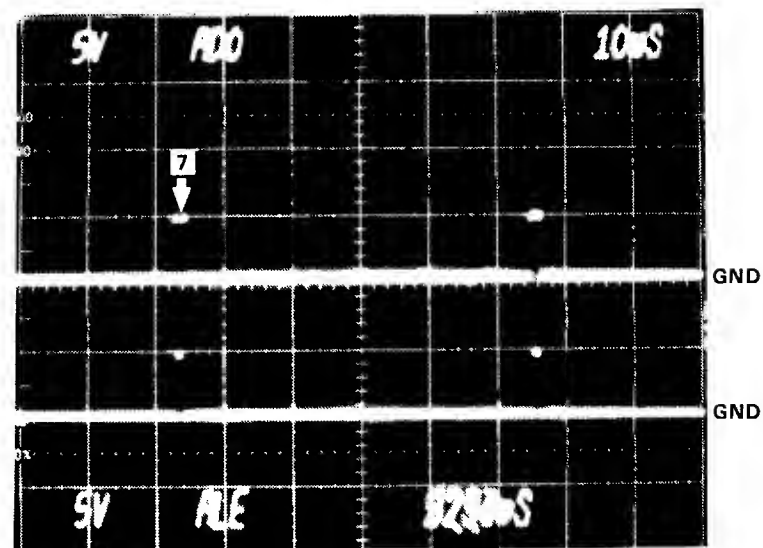
FAMILY CODE 47

Sheet 1 of 2

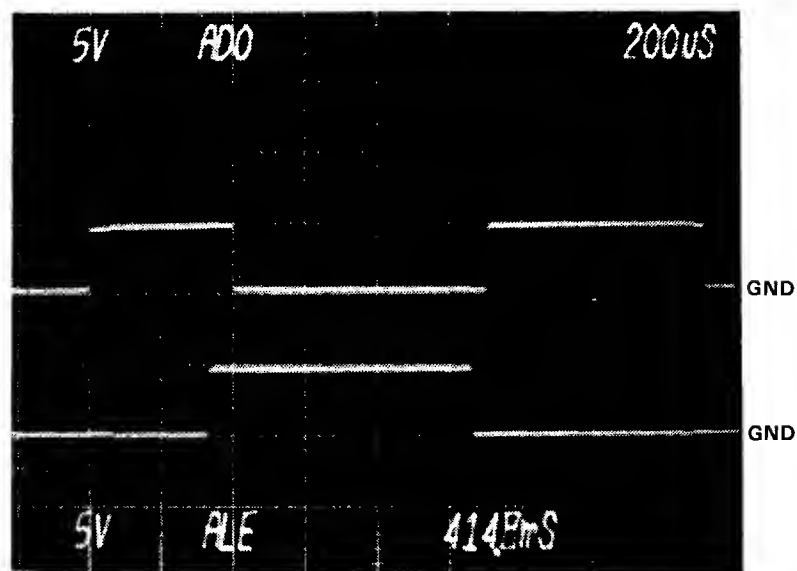
**DATA I/O**



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REVISIONS

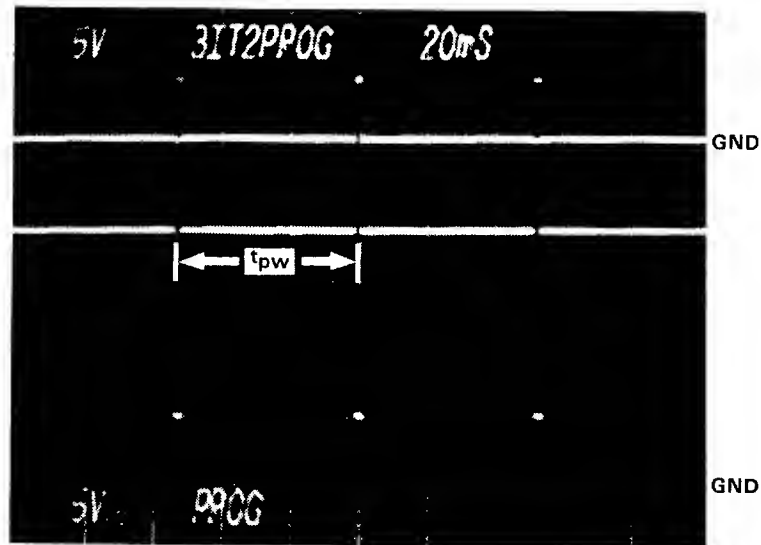
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

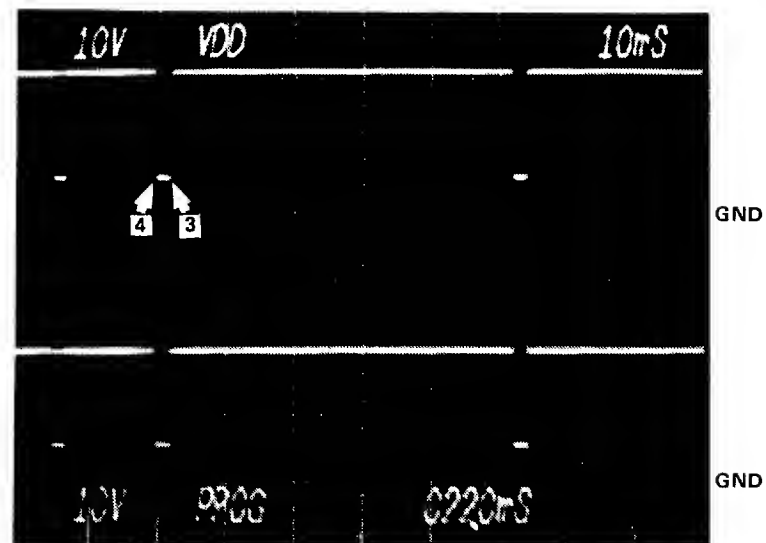
FAMILY CODE 47

Sheet 2 of 2 **DATA I/O**

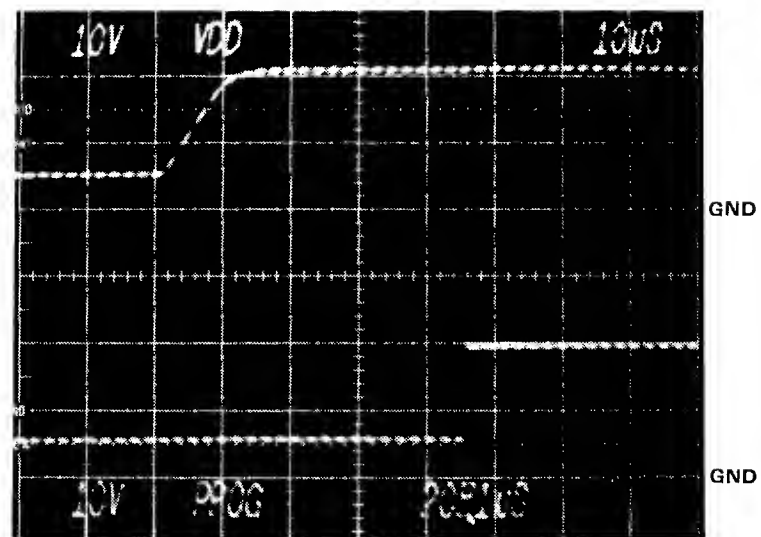




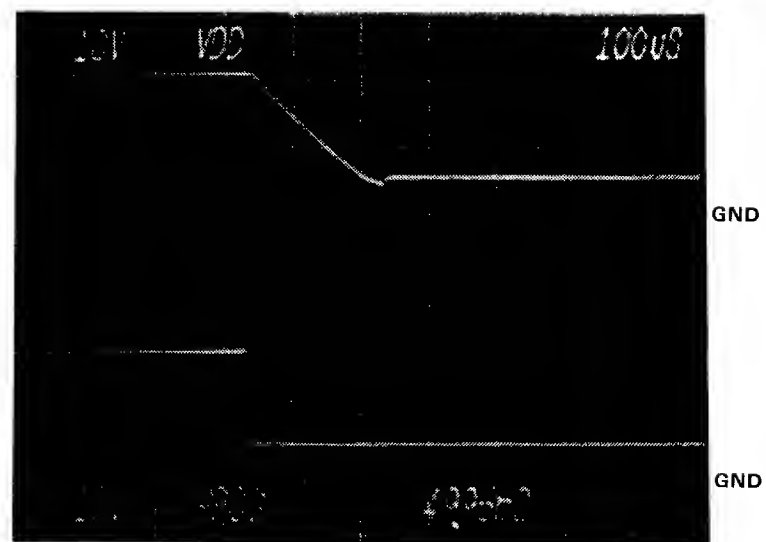
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown
	V <sub>DDV</sub>	4.75	5.00	5.25	V	NA
	PROG,EA	17.5	18.0	18.5	V	EA Not Shown
	V <sub>DDP</sub>	20.5	21.0	21.5	V	
	t <sub>pw</sub>	50		60	ms	
	t <sub>r</sub>	.5			μs	
	t <sub>f</sub>	.5			μs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	4.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>				V	NA
VERIFY	V <sub>REF</sub>				V	NA
	High Load				V	NA
	Low Load				V	NA

## NOTES

1. Load RAM with \$01.

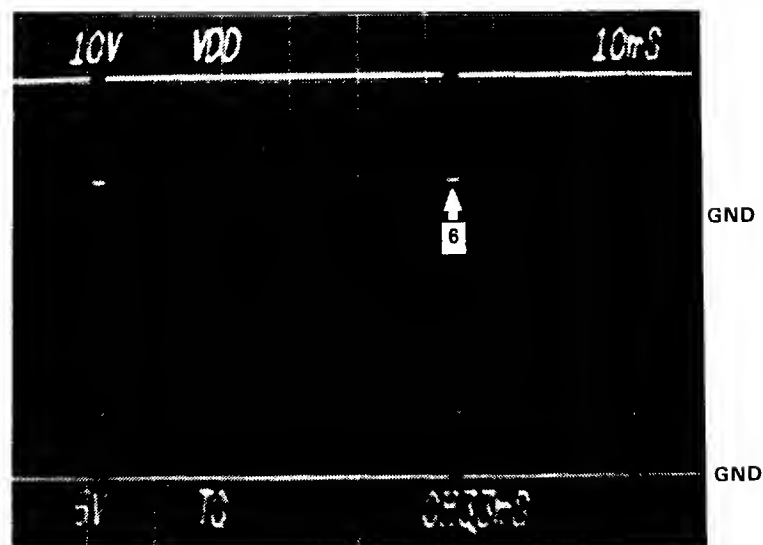
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RJ	5/25/83

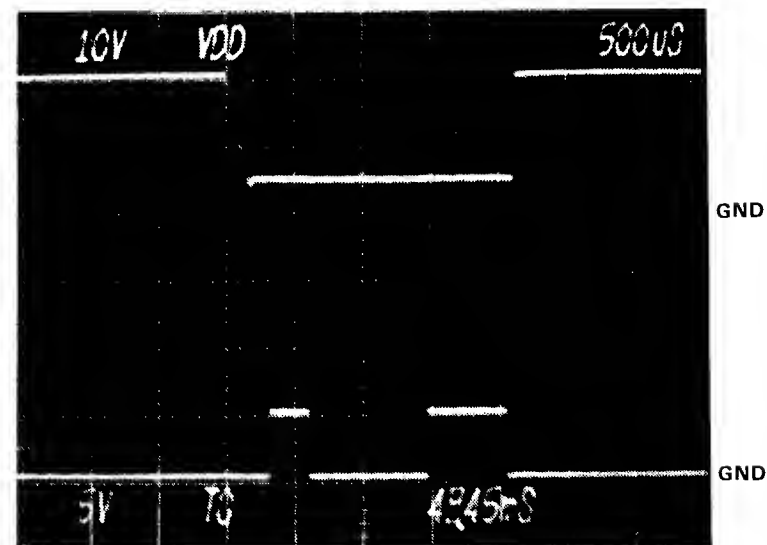
TIMING DIAGRAM

FAMILY CODE 50

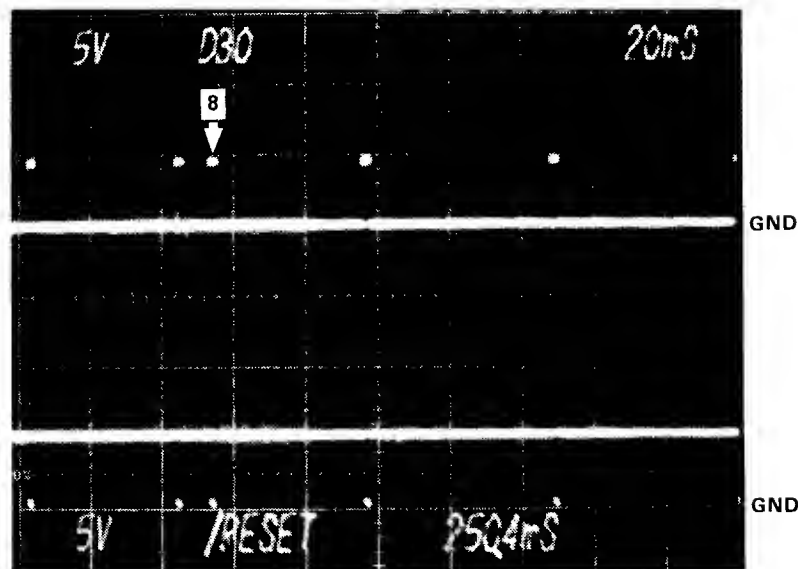
Sheet 1 of 2 **DATA I/O**



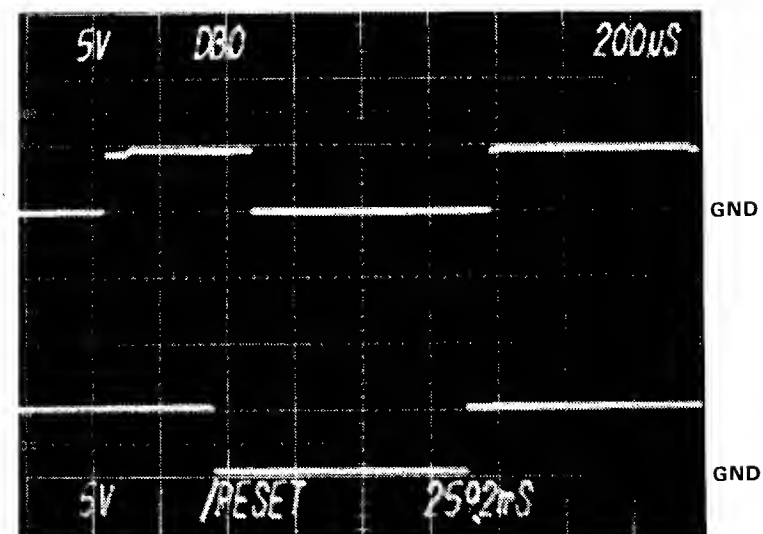
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# REVISIONS

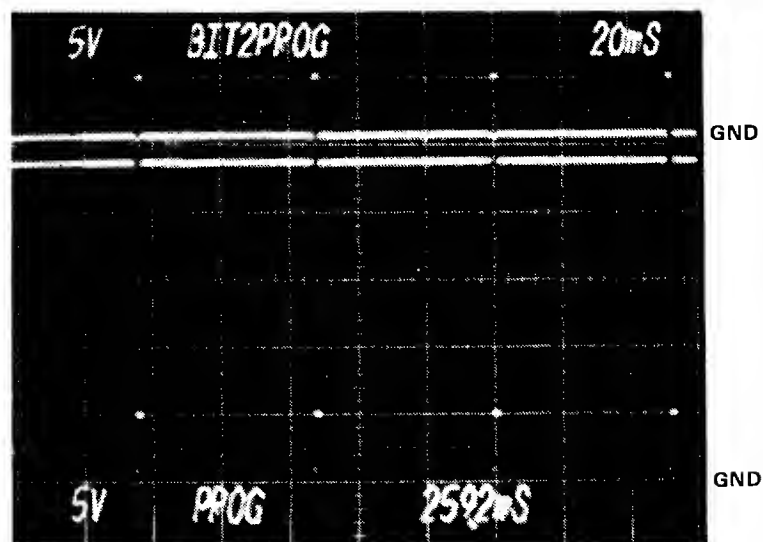
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

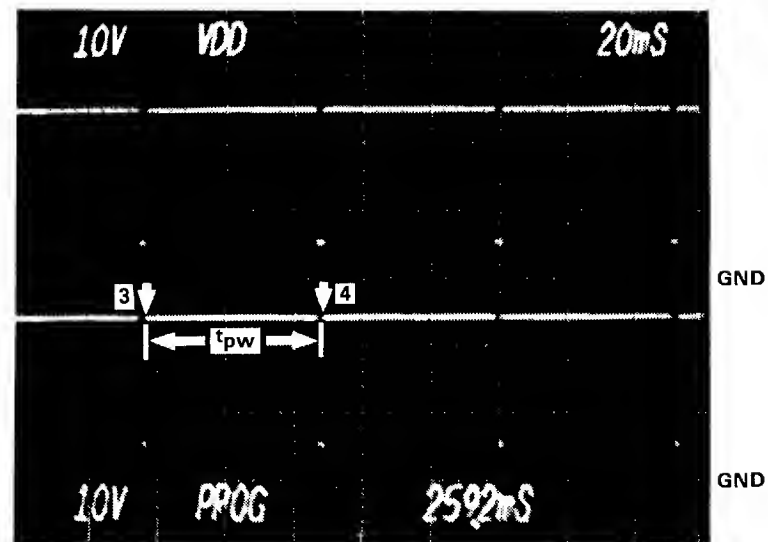
FAMILY CODE 50

Sheet 2 of 2

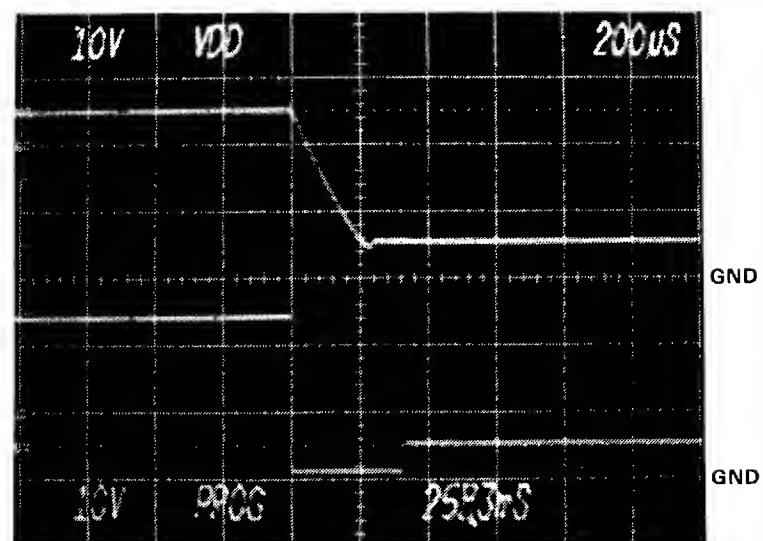
**DATA I/O**



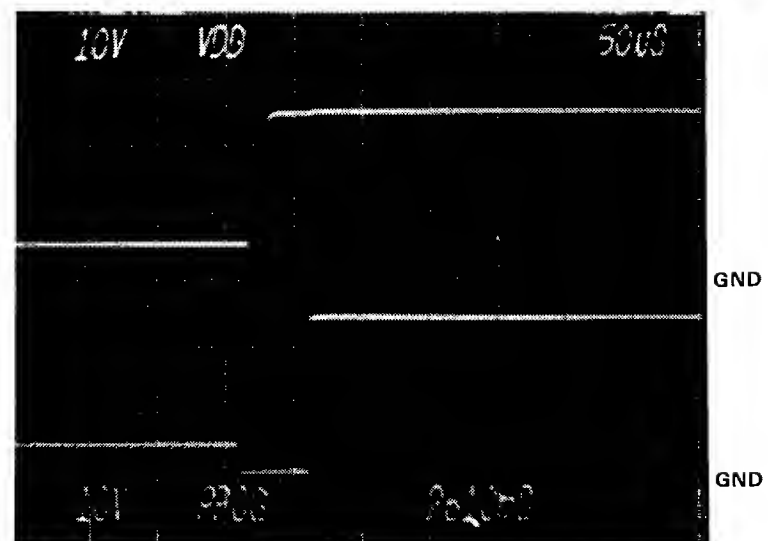
1



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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	
	V <sub>PPV</sub>	4.75	5.00	5.25	V	NA
	PROG,EA	21.5	23.0	24.5	V	EA Not Shown
	V <sub>DDP</sub>	24.0	25.0	26.0	V	
	t <sub>pw</sub>	50		60	ms	
	t <sub>r</sub>	.5			μs	
	t <sub>f</sub>	.5			μs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>				V	NA
VERIFY	V <sub>REF</sub>				V	NA
	High Load				V	NA
	Low Load				V	NA

## NOTES

1. Load RAM with \$01.

## REVISIONS

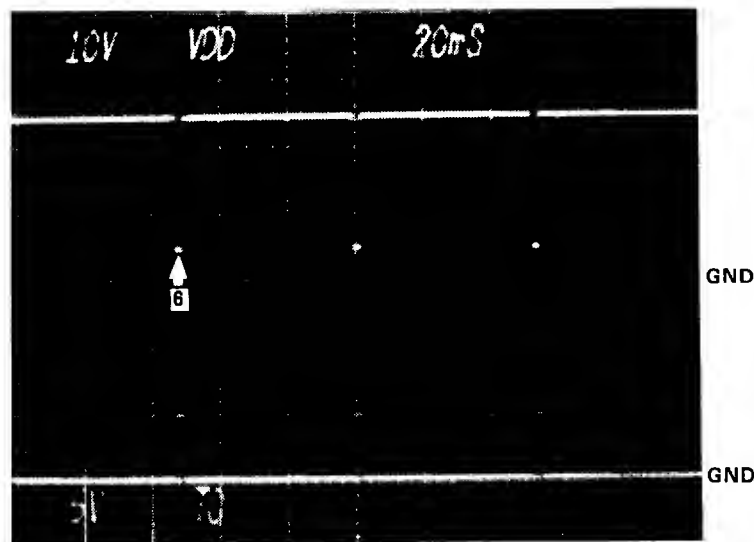
LTR	DESCRIPTION	P.E.	DATE
A	Release	RLL	5/25/83

TIMING DIAGRAM

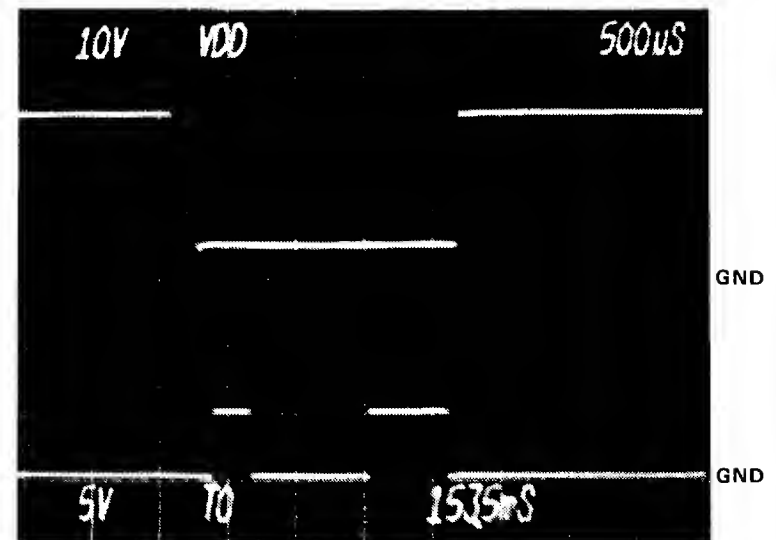
FAMILY CODE 52

Sheet 1 of 2

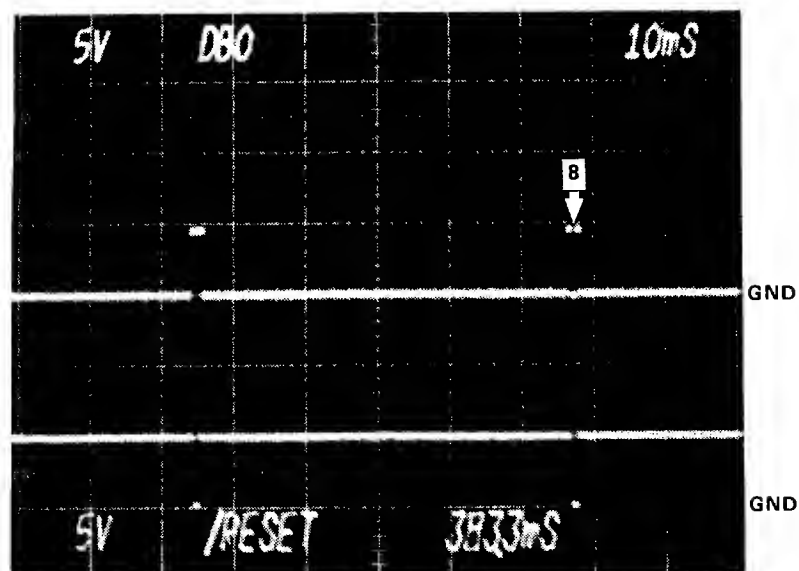
**DATA I/O**



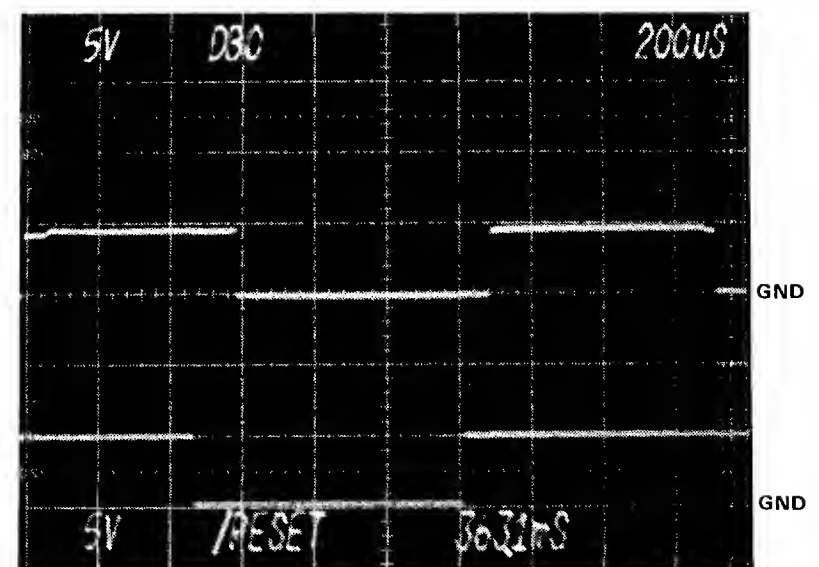
5



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# REVISIONS

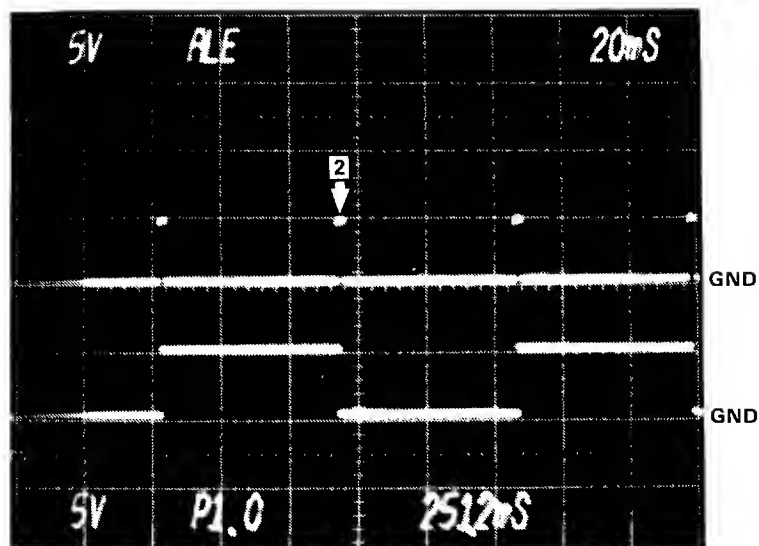
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

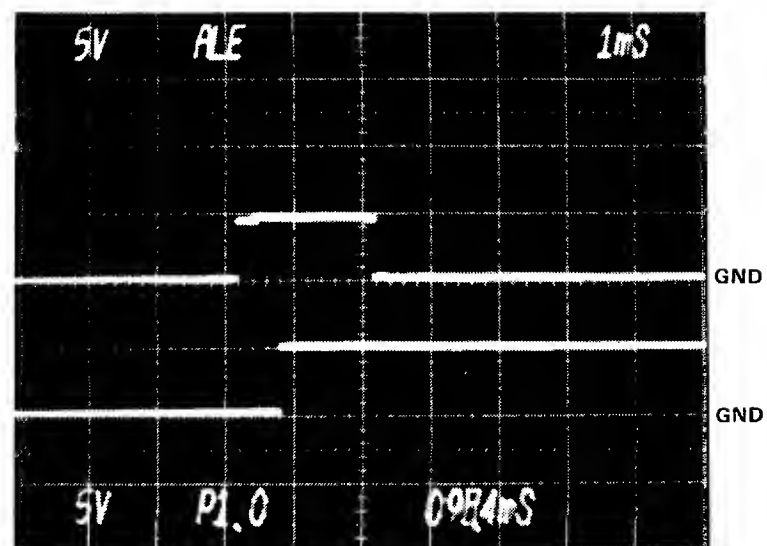
FAMILY CODE 52

Sheet 2 of 2 **DATA I/O**

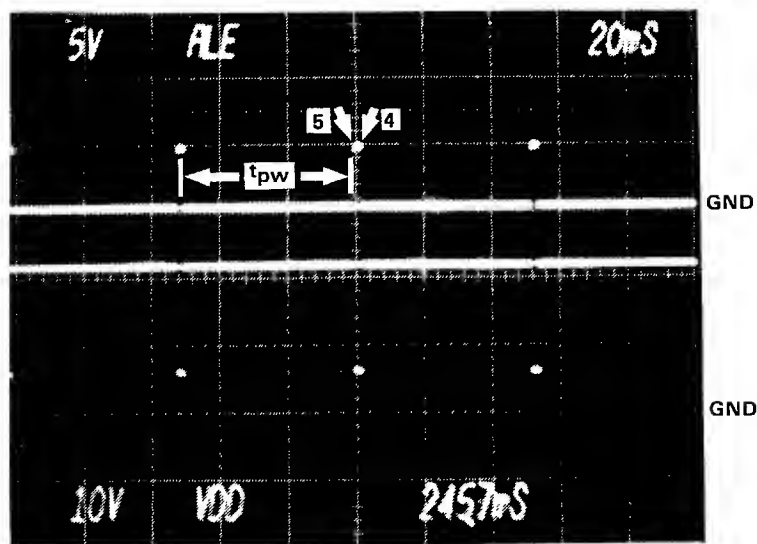




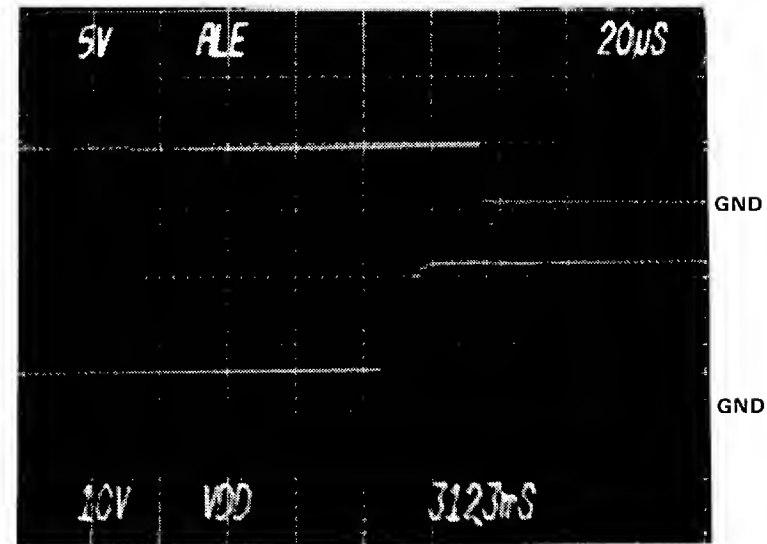
1



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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	Not Shown
	V <sub>OP</sub>					NA
	V <sub>PP</sub>					NA
	V <sub>DD</sub>	20.5	21.0	21.5	V	
	t <sub>pw</sub>	49	50	51	ms	
	t <sub>r</sub>				μs	NA
	t <sub>f</sub>				μs	NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>				V	NA
VERIFY	V <sub>REF</sub>				V	NA
	High Load				V	NA
	Low Load				V	NA

## NOTES

1. Load RAM with \$FE.

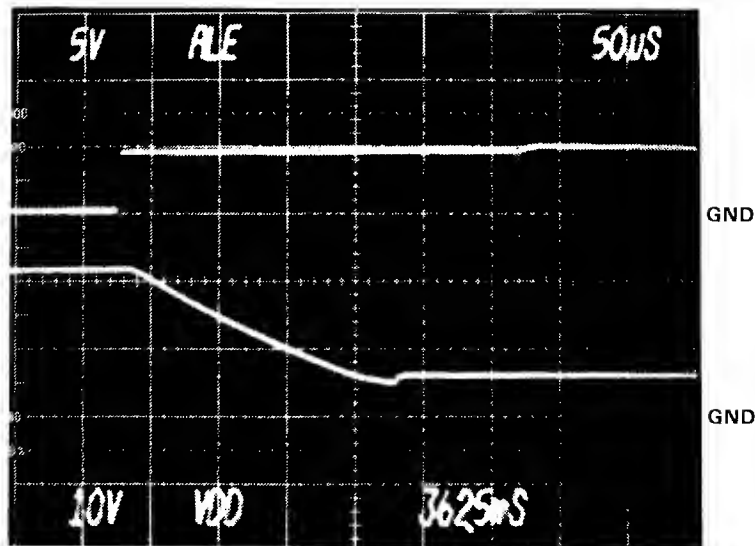
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	REB	5/2/83

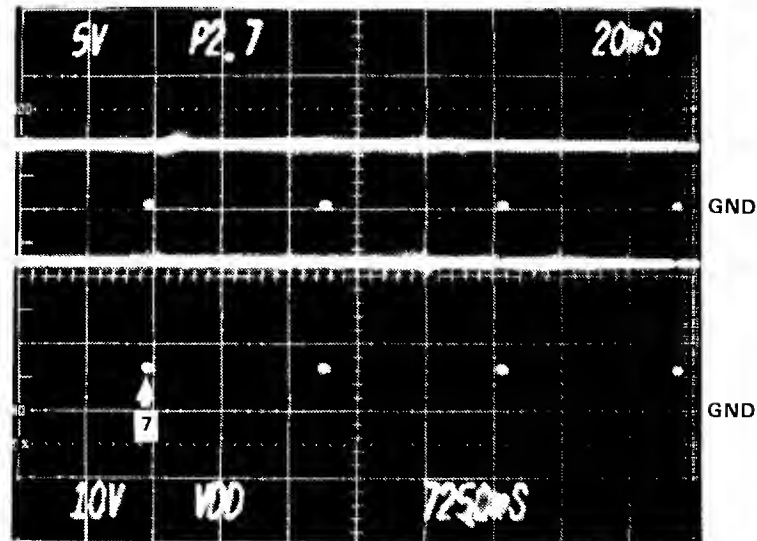
TIMING DIAGRAM

FAMILY CODE 53

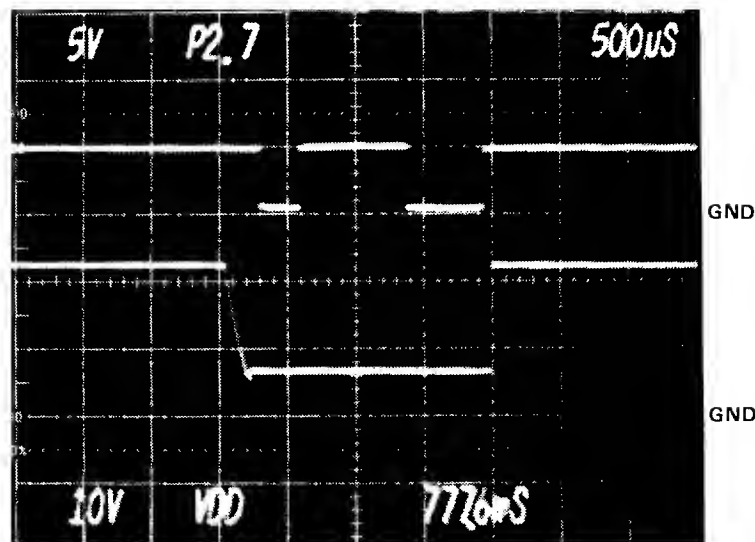
Sheet 1 of 2 **DATA I/O**



5



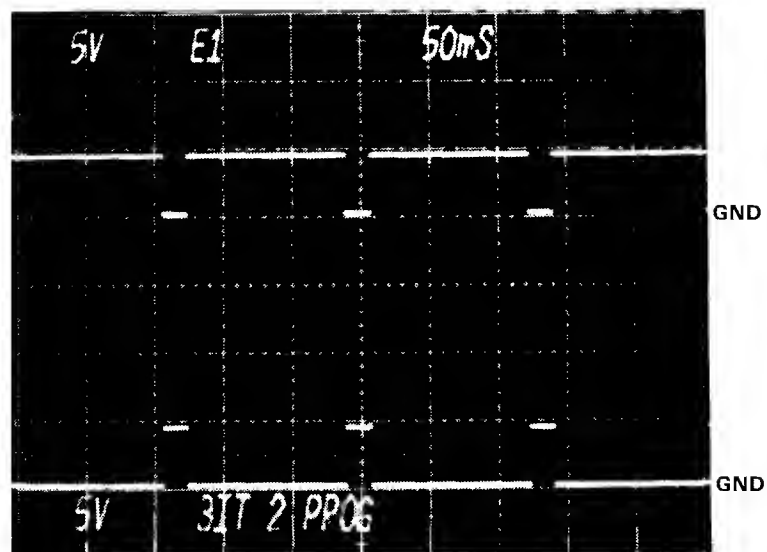
6



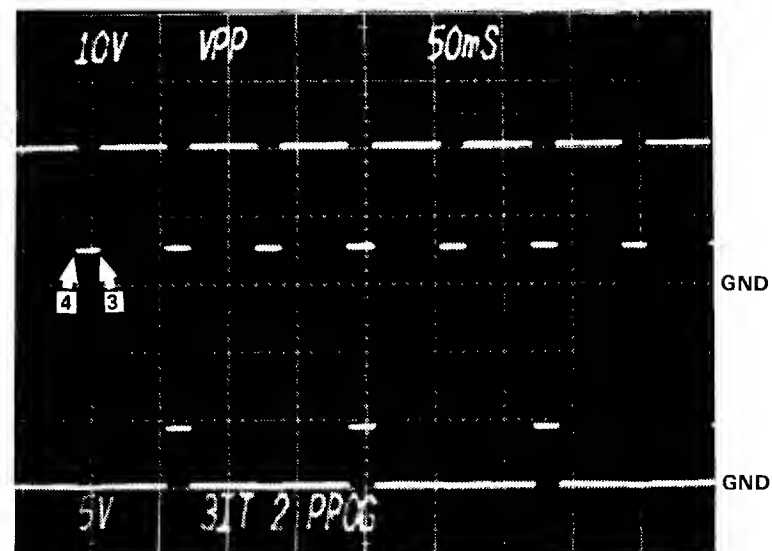
7

REVISIONS

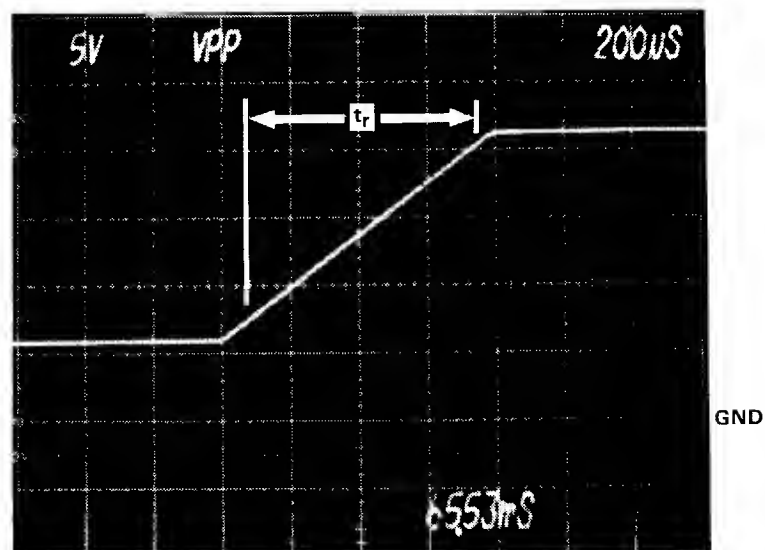
LTR	DESCRIPTION	P.E.	DATE	<div>TIMING DIAGRAM</div> <div>FAMILY CODE 53</div> <div>Sheet 2 of 2 <b>DATA I/O</b></div>
	See Sheet 1			



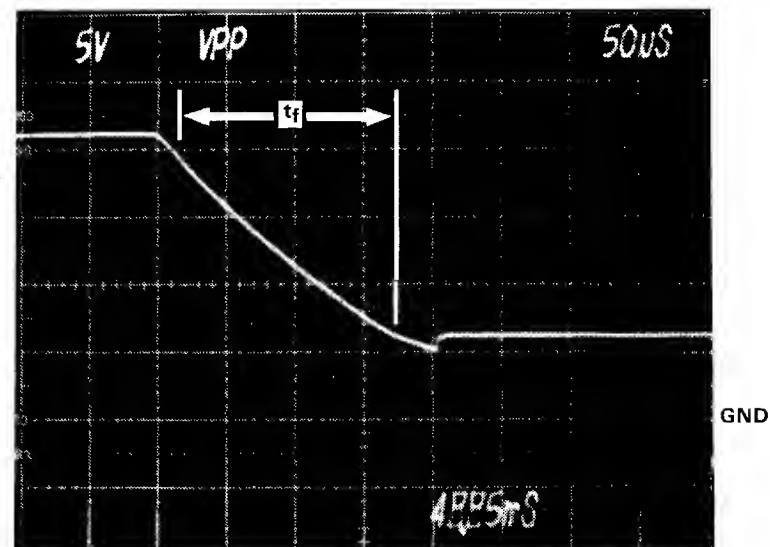
1



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4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.5	5.8	6.1	V	Not Shown
	V <sub>PP</sub>	20.0	20.5	21.0	V	
	V <sub>PPN</sub>	5.7	5.9	6.1	V	
	t <sub>pw</sub>	45	50	55	ms	
	t <sub>r</sub>	50			μs	
	t <sub>f</sub>	50			μs	
	Reject		4		Pulses	
	Overprogram		1		Pulses	See note 2
1ST PASS VERIFY	V <sub>CC</sub>	4.8	4.9	5.0	V	
	V <sub>REF</sub>	0.7	0.8	0.9	V	702-1775/TP18
	High Load	0.0	0.0	0.4	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	5.4	5.5	5.6	V	
	V <sub>REF</sub>	3.4	3.5	3.6	V	702-1775/TP18
	High Load	0.0	0.0	0.4	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. Pulse 2 of the 4 pulse string is actually an overprogram pulse.

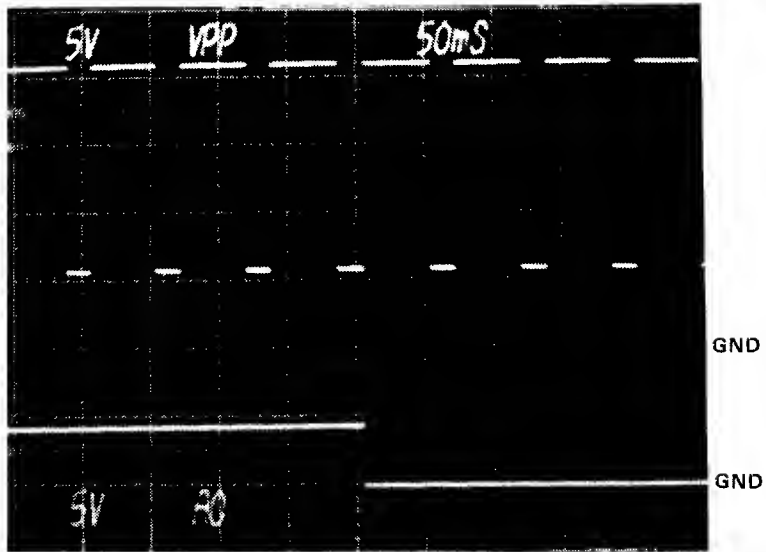
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	R22	5/25/83

TIMING DIAGRAM

FAMILY CODE 59

Sheet 1 of 2 **DATA I/O**



REVISIONS

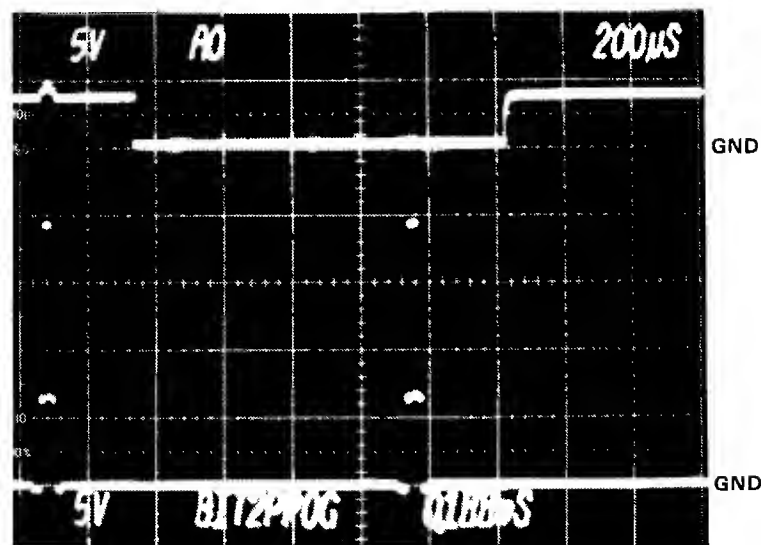
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

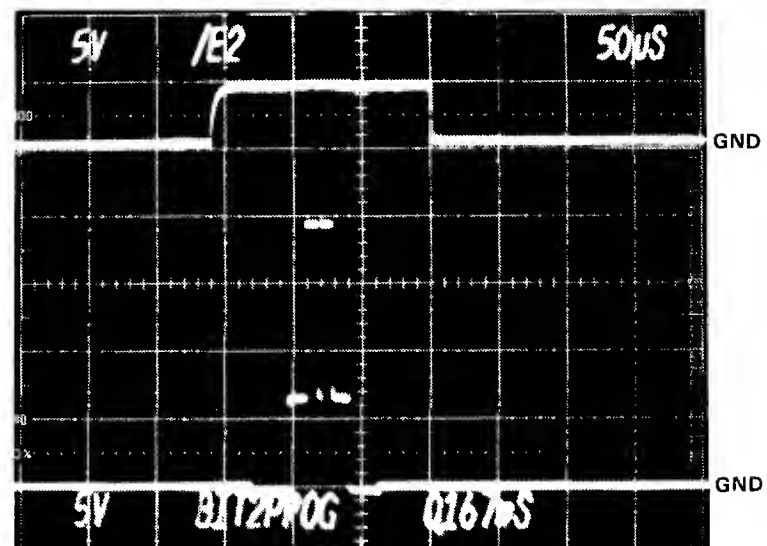
FAMILY CODE 59

Sheet 2 of 2 **DATA I/O**

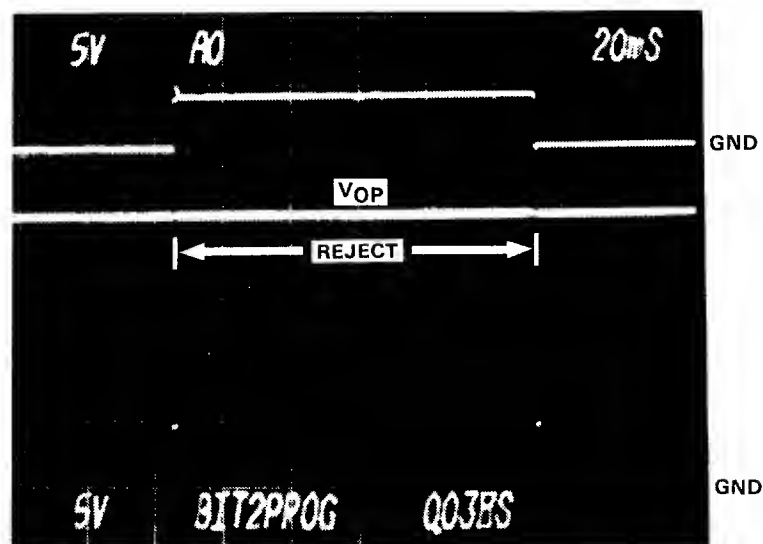




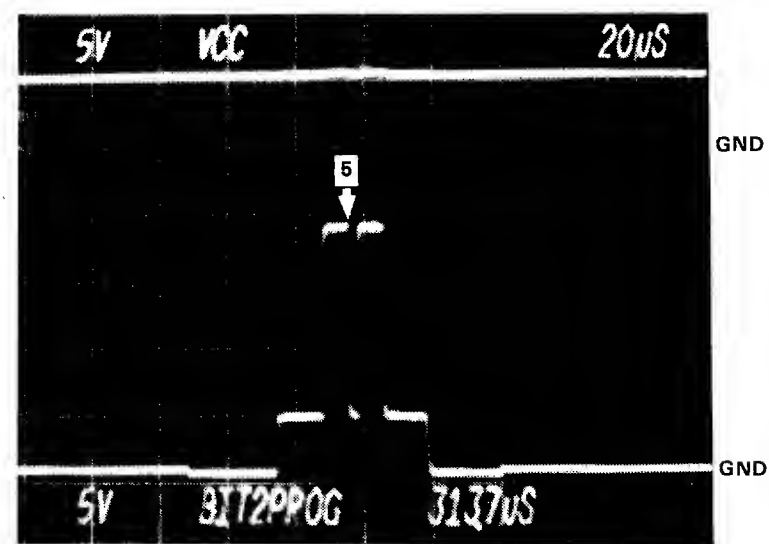
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.00	5.25	V	
	V <sub>OP</sub>	19.0	19.5	20.0	V	
	t <sub>pw</sub>	7.0	7.5	8.0	ms	See note 4
	t <sub>r</sub>	0.21		0.30	μs	
	t <sub>f</sub>	0.21		0.30	μs	
	Overprogram		1		Pulses	
	Reject		10000		Pulses	See note 5
	Duty Cycle	70	75	80	%	
1ST PASS	V <sub>CC</sub>	4.5	4.6	4.7	V	
VERIFY	V <sub>REF</sub>	0.7	0.8	0.9	V	702-1775/TP18
	High Load	17.5	18.0	18.5	V	702-1775/TP15
	Low Load	17.5	18.0	18.5	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	6.5	6.6	6.7	V	
VERIFY	V <sub>REF</sub>	4.4	4.5	4.6	V	702-1775/TP18
	High Load		0.0	0.5	V	702-1775/TP15
	Low Load	5.6	5.7	5.8	V	702-1775/TP14

## NOTES

1. Fill RAM with \$01.
2. Use a 200Ω Id. on Bit to Program for all waveforms except Photo #3. Photo #3 should have no load on BTP.
3. Do not use a wirewound Id. resistor.
4. Measurement taken at 10V point of 01 with a 200Ω Id.
5. 10,000 pulses equals 100 ms as shown in photo #3.

## REVISIONS

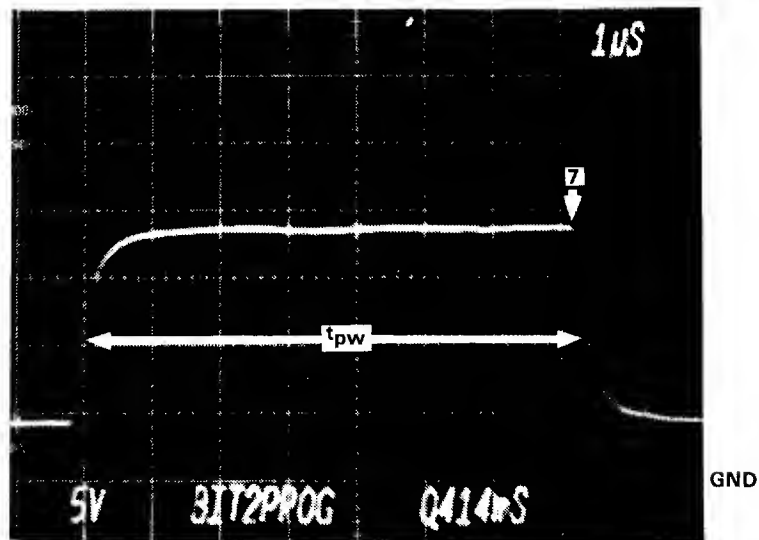
LTR	DESCRIPTION	P.E.	DATE
A	Release	REL	5/25/83

TIMING DIAGRAM

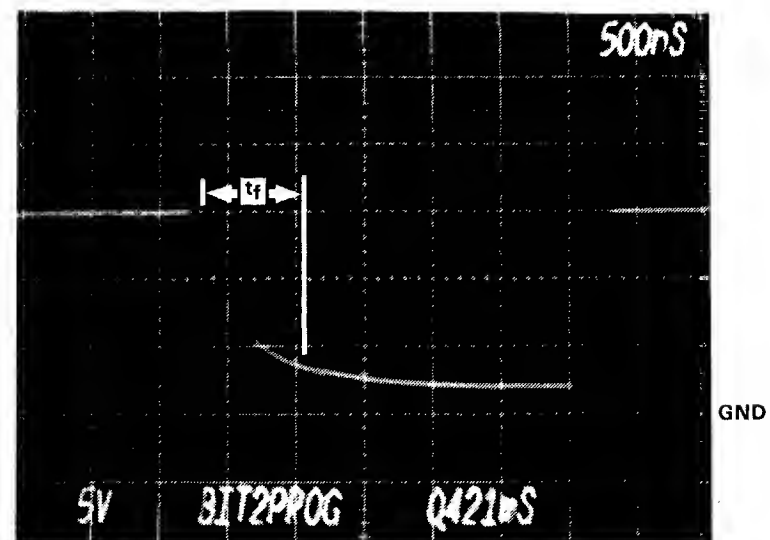
FAMILY CODE 66

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# DATA I/O



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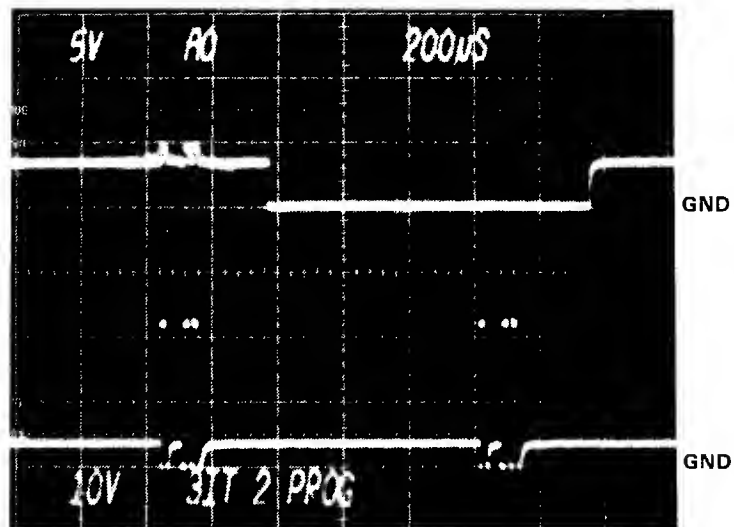
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

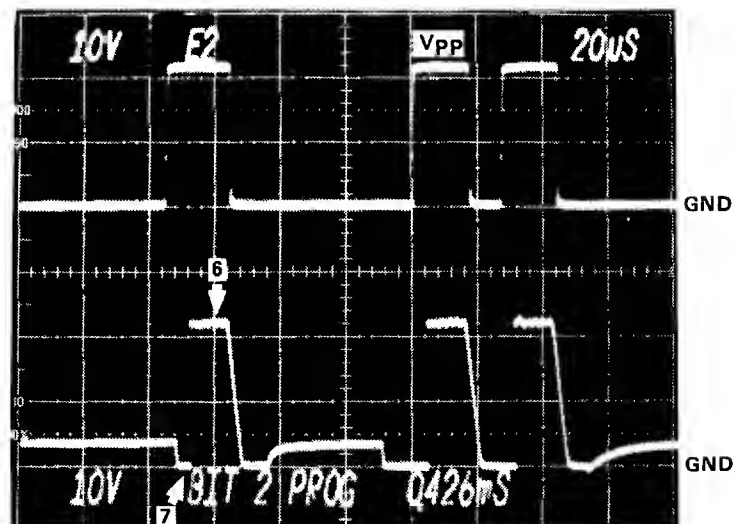
TIMING DIAGRAM

FAMILY CODE 66

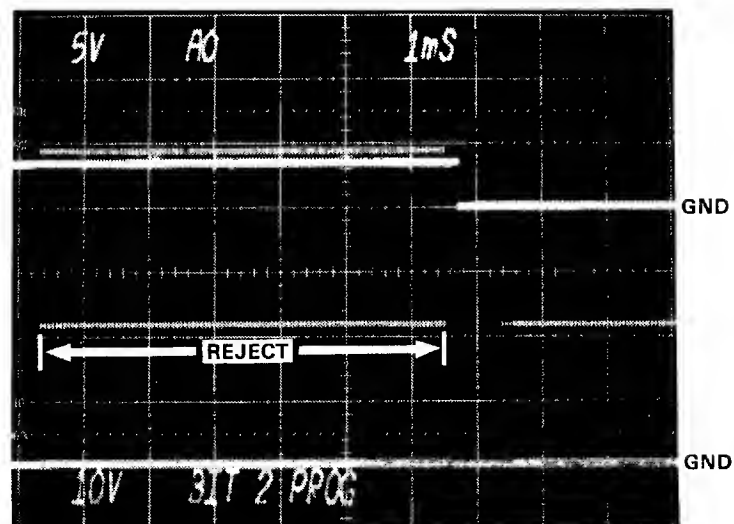
Sheet 2 of 2 **DATA I/O**



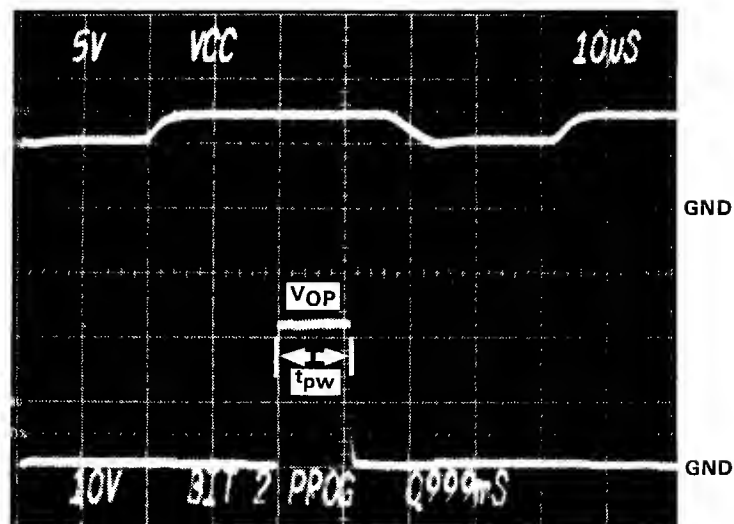
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	6.7	7.0	7.5	V	
	V <sub>PP</sub>	20.0	21.0	22.0	V	
	V <sub>OP</sub>	20.0	21.0	22.0	V	
	t <sub>pw</sub>	10.0	11.0	12.0	μs	See Note 2
	t <sub>r</sub>			2.0	μs	
	t <sub>f</sub>			2.0	μs	
	Overprogram		2		Pulses	
	Reject		100		Pulses	See Note 3
	Duty Cycle	15	20	25	%	
1ST PASS	V <sub>CC</sub>	4.0	4.1	4.2	V	
VERIFY	V <sub>REF</sub>	0.7	0.8	0.9	V	702-1775/TP18
	High Load	17.5	18.0	18.5	V	702-1775/TP15
	Low Load	17.5	18.0	18.5	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	6.9	7.0	7.1	V	
VERIFY	V <sub>REF</sub>	3.9	4.0	4.1	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	5.0	5.4	5.8	V	702-1775/TP14

## NOTES

1. Fill RAM with \$01.
2. Measurement taken at 15V point of 01 with a 200Ω load.
3. 100 pulses equally 6.4 ms as shown in photo number 3.
4. V<sub>CC</sub> loaded with 330Ω resistor as shown in photo 5.
5. Do not use a wirewound load resistor.
6. 01 is loaded with 200Ω resistor in all photos except 1 and 2.
7. Photos 1 and 2 not loaded.

## REVISIONS

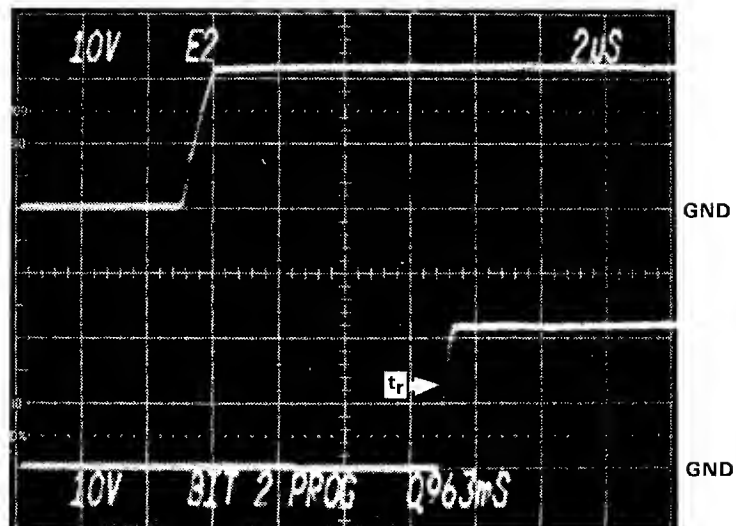
LTR	DESCRIPTION	P.E.	DATE
A	Release	R23	5/25/83

TIMING DIAGRAM

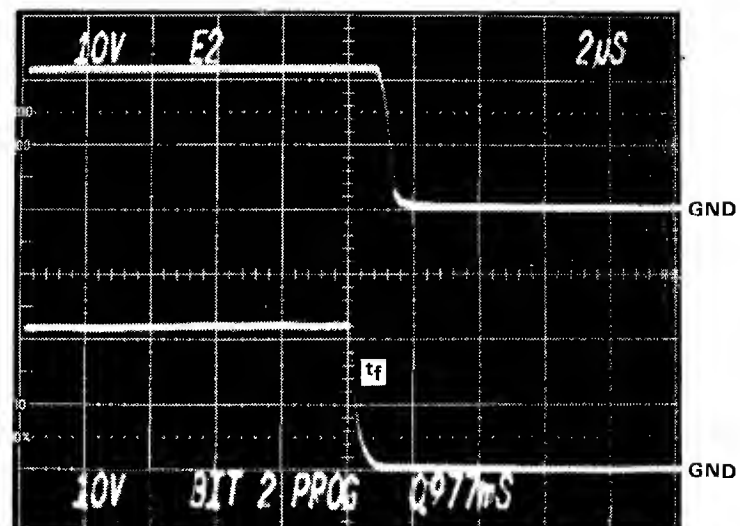
FAMILY CODE 68

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# DATA I/O



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# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

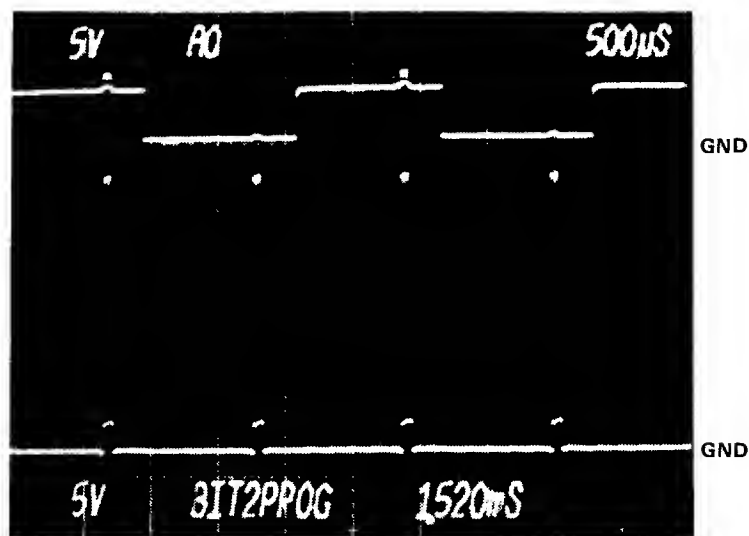
TIMING DIAGRAM

FAMILY CODE 68

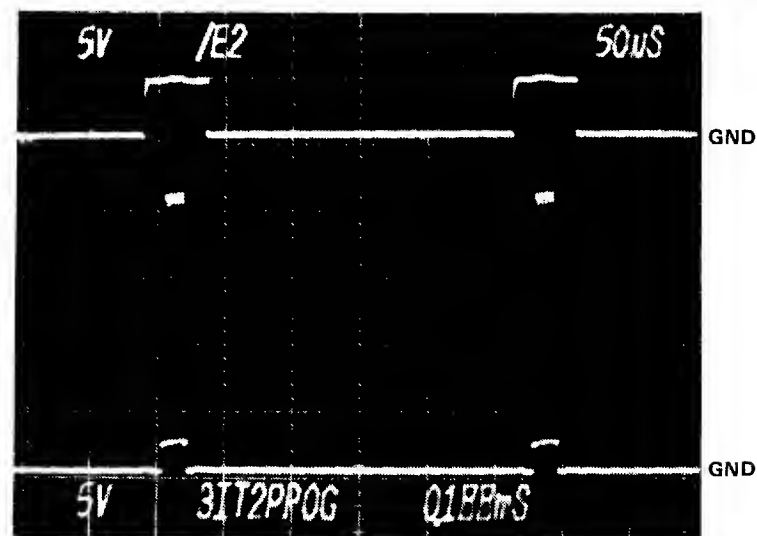
Sheet 2 of 2

**DATA I/O**

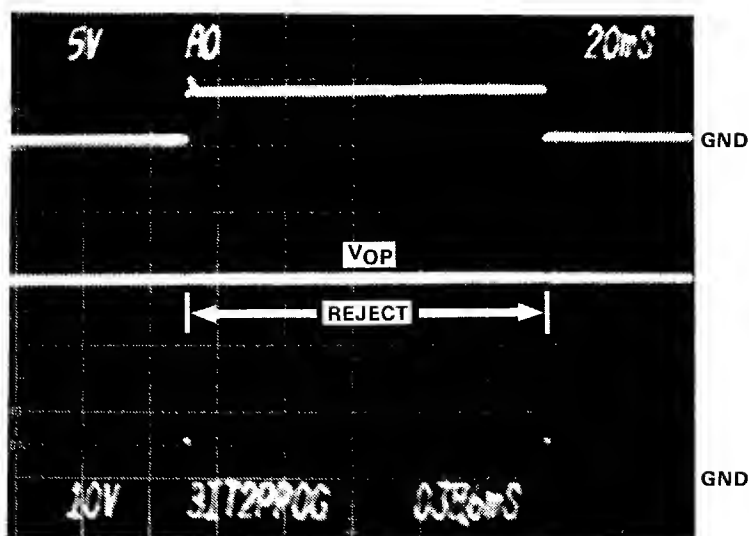




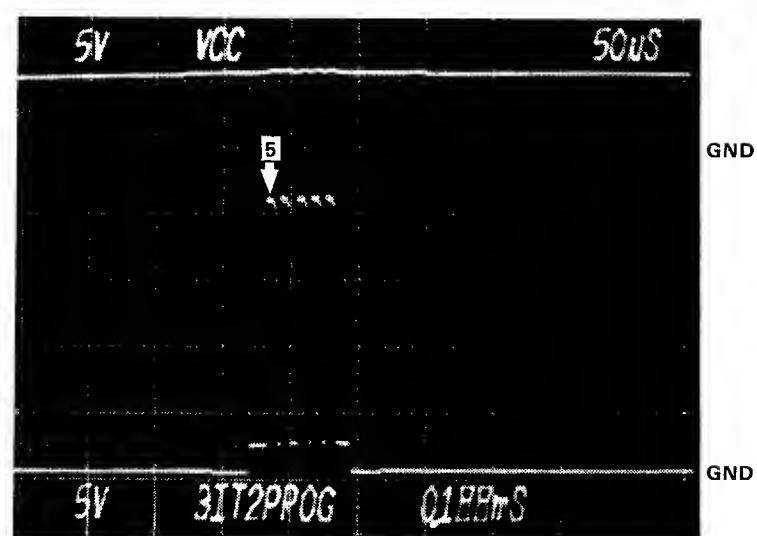
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	NA
	VPP					
	VOP	27.5	28.0	28.5	V	
	t <sub>pw</sub>	7.0	7.5	8.0	μs	See Note 2
	t <sub>r</sub>	0.21		0.30	μs	
	t <sub>f</sub>	0.21		0.30	μs	
	Overprogram		4		Pulses	See Note 3
	Reject		10000		Pulses	
	Duty Cycle	70	75	80	%	
1ST PASS	VCC	4.0	4.1	4.2	V	
VERIFY	VREF	0.7	0.8	0.9	V	702-1775/TP18
	High Load	17.5	18.0	18.5	V	702-1775/TP15
	Low Load	17.5	18.0	18.5	V	702-1775/TP14
2ND PASS	VCC	6.4	6.5	6.6	V	
VERIFY	VREF	4.2	4.3	4.4	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	5.4	5.7	6.0	V	702-1775/TP14

## NOTES

1. Fill RAM with \$01.
2. Measurement taken at 10V point of 01.
3. 100,000 pulses equals 100 ms as shown in photo number 3.
4. Do not use a wirewound load resistor.
5. Use 100Ω load resistor on bit-to-program for all waveforms except for photo #3. Photo #3 should have no load on bit-to-program.

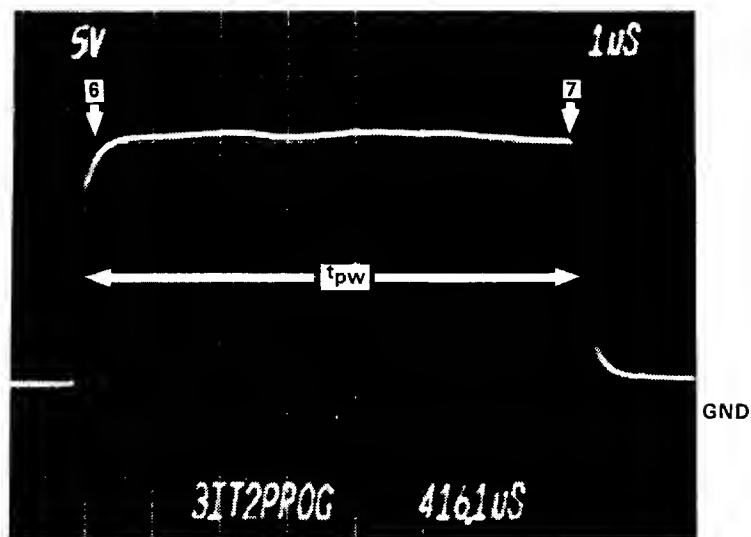
## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RJS	5/25/83

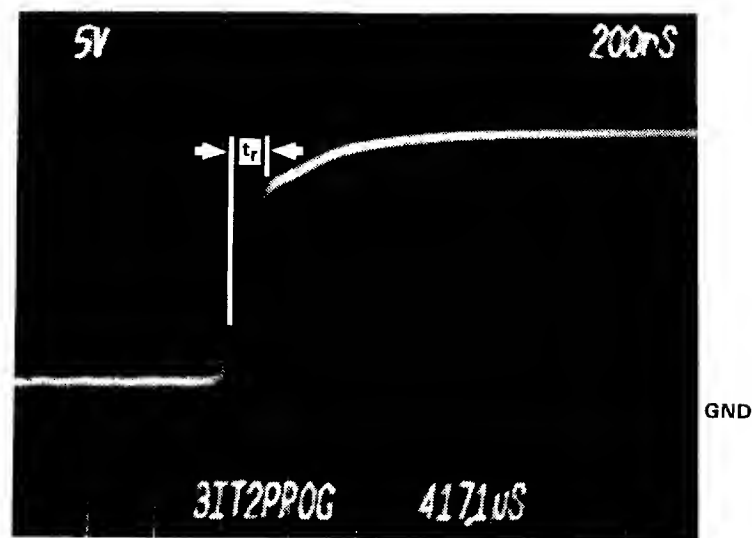
TIMING DIAGRAM

FAMILY CODE 70

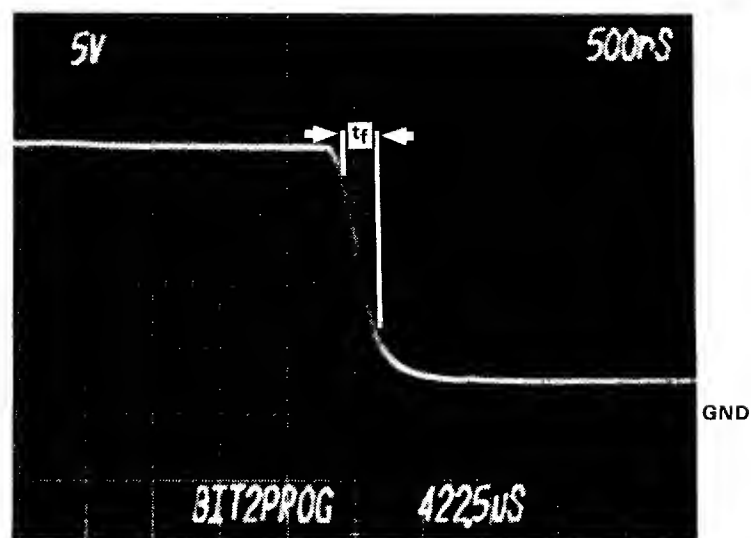
Sheet 1 of 2 **DATA I/O**



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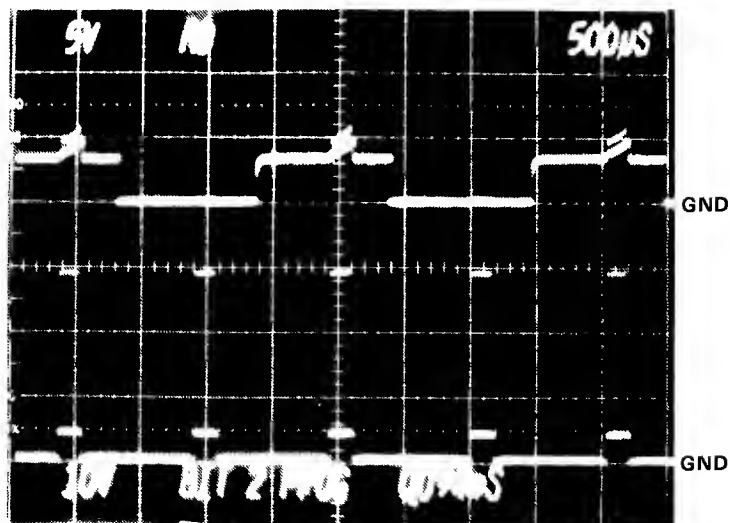
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

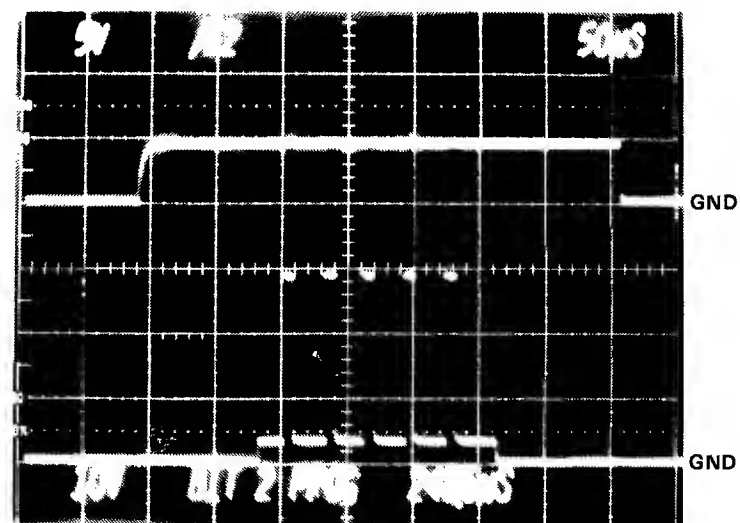
TIMING DIAGRAM

FAMILY CODE 70

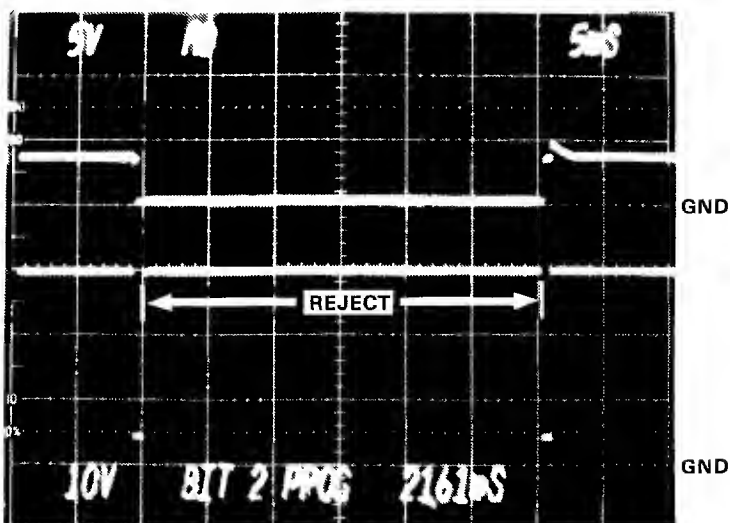
Sheet 2 of 2 **DATA I/O**



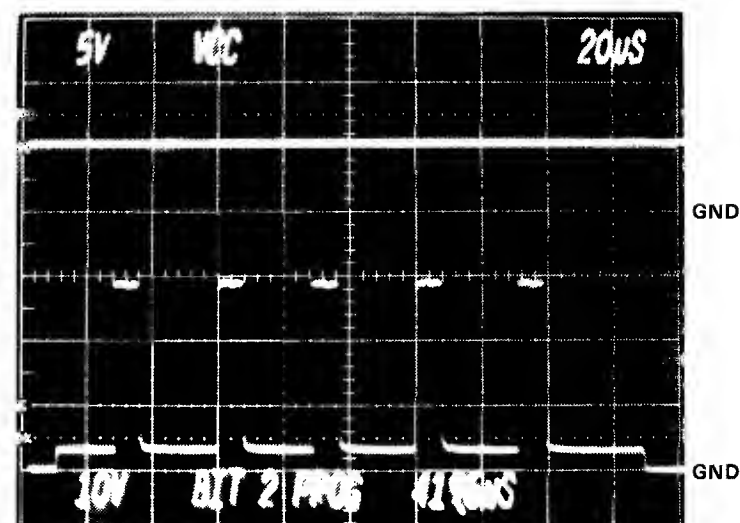
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# REVISIONS

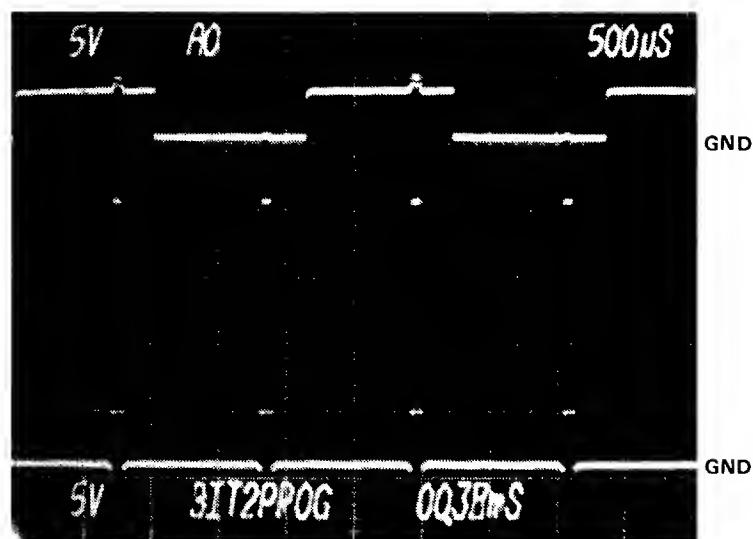
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

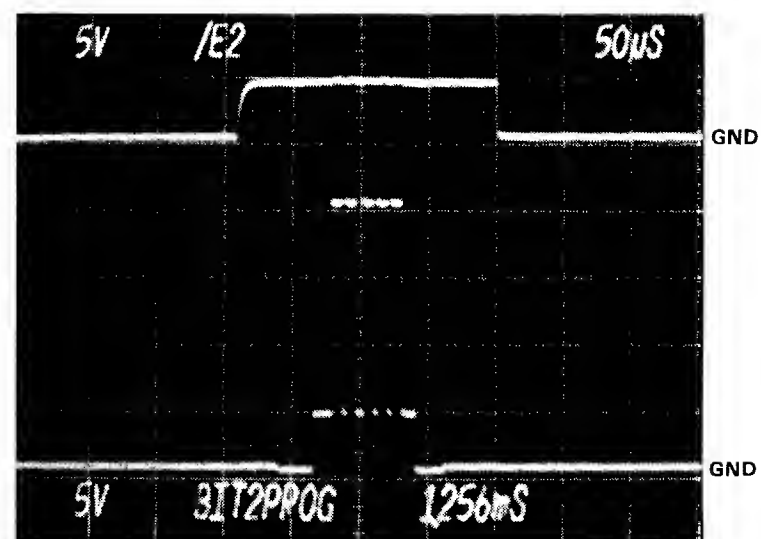
FAMILY CODE 72

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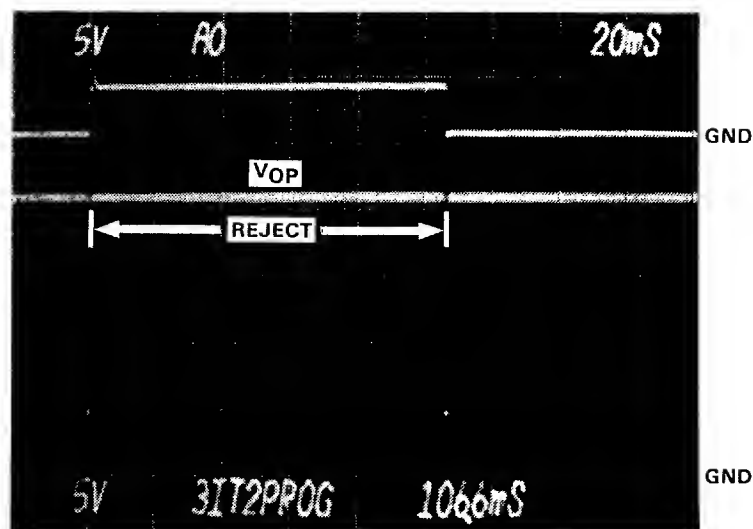
**DATA I/O**



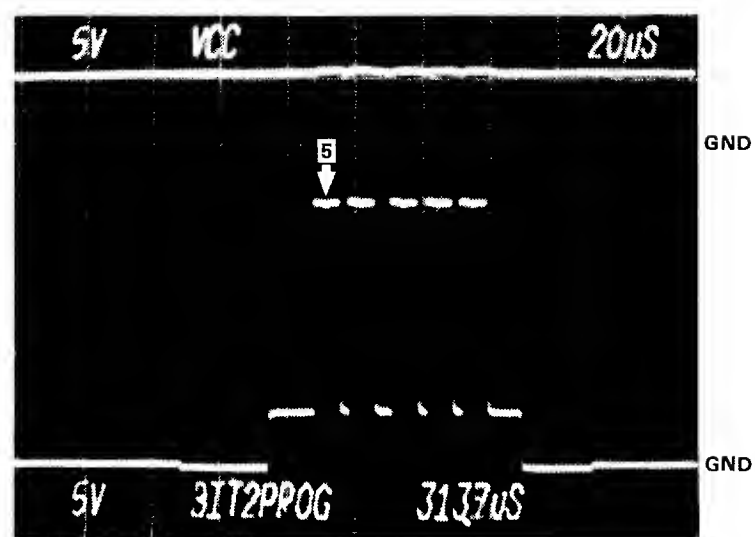
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.8	5.1	5.3	V	NA
	V <sub>pp</sub>					
	V <sub>OP</sub>	19.3	19.8	20.3	V	
	t <sub>pw</sub>	7.0	7.5	8.0	μs	See note 4
	t <sub>r</sub>	0.21		0.30	μs	
	t <sub>f</sub>	0.21		0.30	μs	
	Overprogram		4		Pulses	See note 5
	Reject		10000		Pulses	
	Duty Cycle	70	75	80	%	
1ST PASS	V <sub>CC</sub>	4.5	4.6	4.7	V	
VERIFY	V <sub>REF</sub>	.7	.8	.9	V	702-1775/TP18
	High Load	17.5	18.0	18.5	V	702-1775/TP15
	Low Load	17.5	18.0	18.5	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	6.5	6.6	6.7	V	
VERIFY	V <sub>REF</sub>	4.4	4.5	4.6	V	702-1775/TP18
	High Load		0.0	0.5	V	702-1775/TP15
	Low Load	5.4	5.7	6.0	V	702-1775/TP14

## NOTES

1. Load RAM with \$01.
2. Use 200Ω load on BTP for all waveforms except photo #3. Photo #3 should have no load on BTP.
3. Do not use a wirewound load resistor.
4. Measurement taken at 10V point of 01 with a 200Ω Id.
5. 10000 pulses equals 100 ms as shown in photo #3.

## REVISIONS

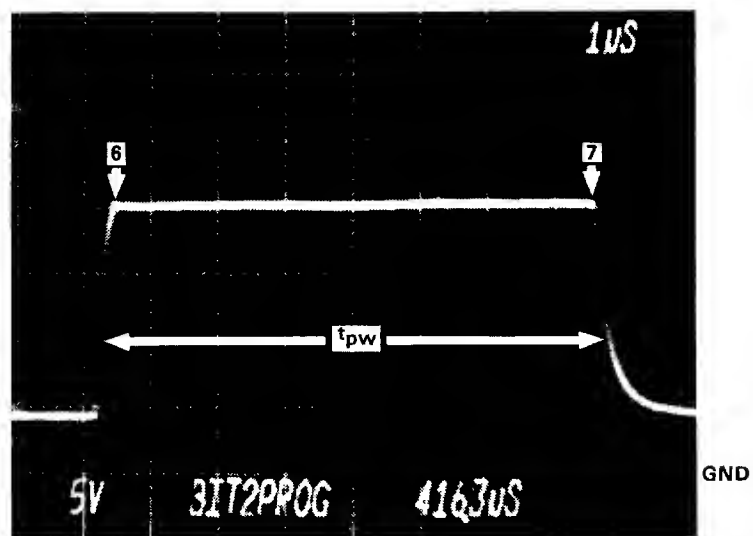
LTR	DESCRIPTION	P.E.	DATE
A	Release	ADD	5/25/03

TIMING DIAGRAM

FAMILY CODE 74

Sheet 1 of 2 **DATA I/O**

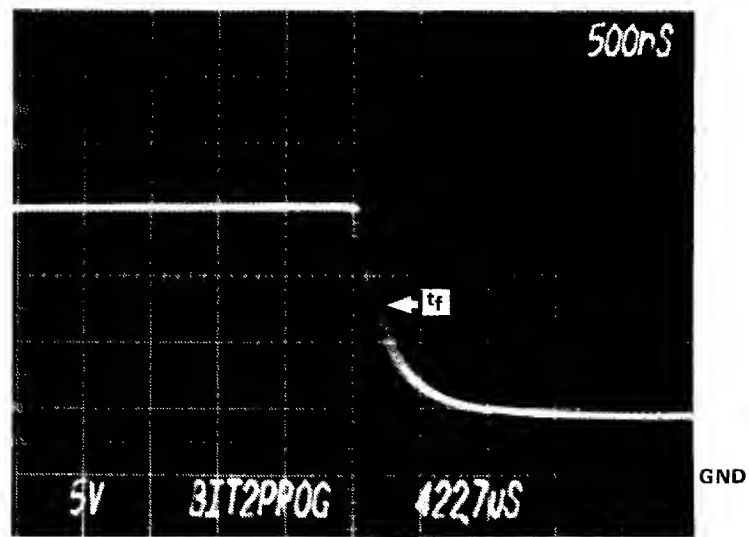




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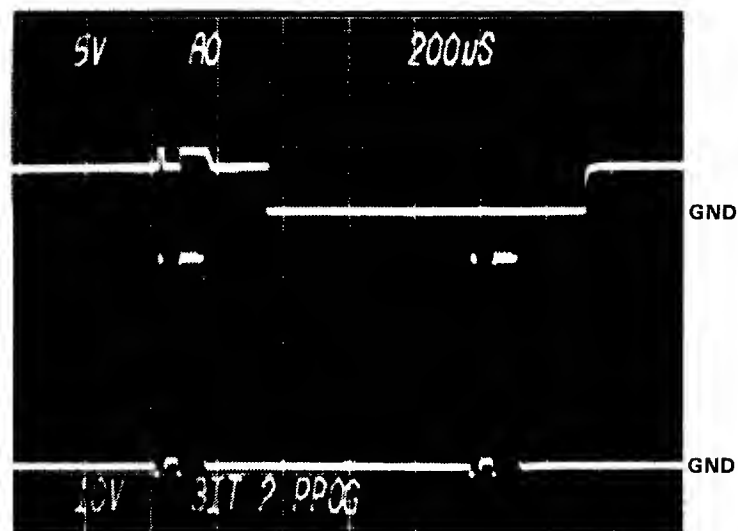
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

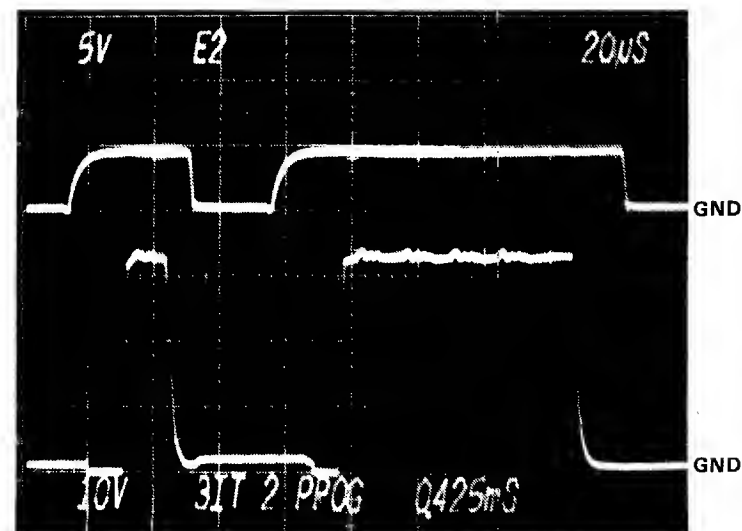
TIMING DIAGRAM

FAMILY CODE 74

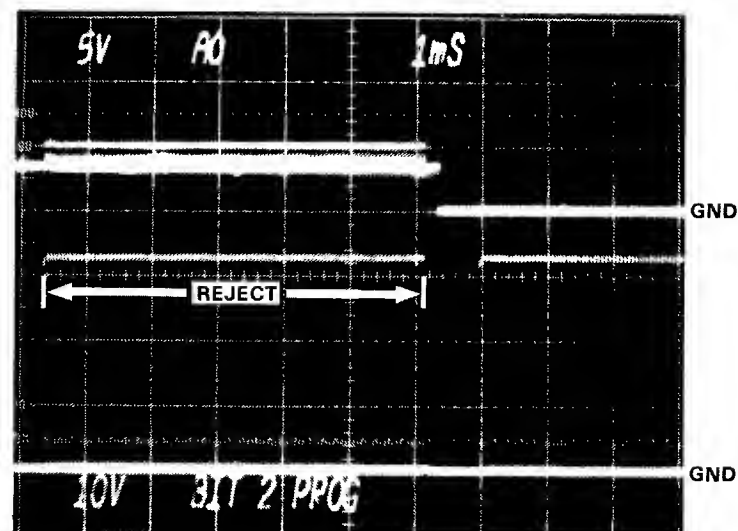
Sheet 2 of 2 **DATA I/O**



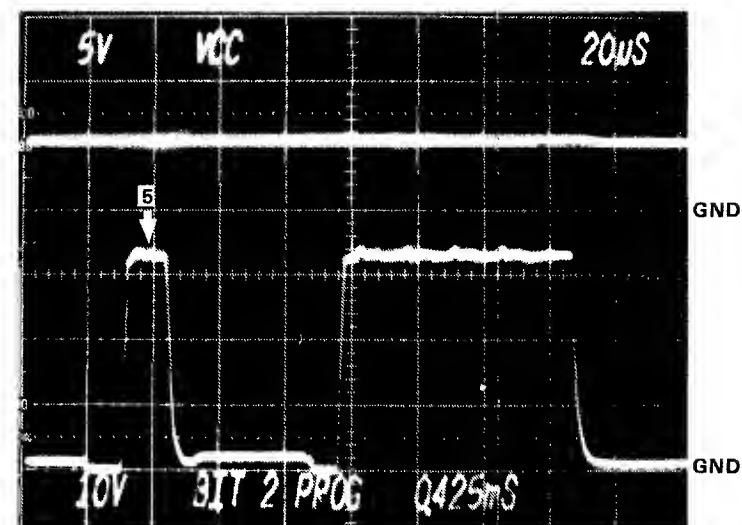
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	NA
	V <sub>PP</sub>					
	V <sub>OP</sub>	31.5	31.7	32.0	V	
	t <sub>pn</sub>	7.2	7.5	7.8	μs	See note 2
	t <sub>r</sub>	0.34		0.48	μs	
	t <sub>f</sub>	0.34		0.48	μs	
	Overprogram		4		Pulses	See note 3
	Reject		100		Pulses	
	Duty Cycle	11			%	
1ST PASS VERIFY	V <sub>CC</sub>	4.4	4.5	4.6	V	
	V <sub>REF</sub>	0.7	0.8	0.9	V	702-1775/TP18
	High Load	17.5	18.0	18.5	V	702-1775/TP15
	Low Load	17.5	18.0	18.5	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	6.4	6.5	6.6	V	
	V <sub>REF</sub>	3.9	4.0	4.1	V	702-1775/TP18
	High Load		0.0	0.5	V	702-1775/TP15
	Low Load	5.4	5.7	6.0	V	702-1775/TP14

## NOTES

1. Load RAM with \$01 for Family 78.
2. Measurement taken at 15v point of 01 with 150Ω load.
3. 100 pulses equals 5.8 ms as shown in photo number 3 with 150Ω load.
4. Do not use a wirewound load resistor.
5. Photos 1, 2, and 4 have 01 loaded with 3.3kΩ.

## REVISIONS

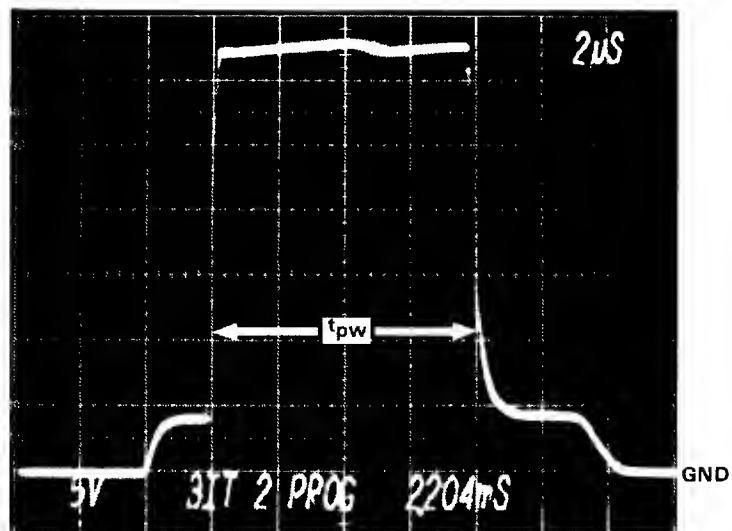
LTR	DESCRIPTION	P.E.	DATE
A	Release	RLB	5/25/03

TIMING DIAGRAM

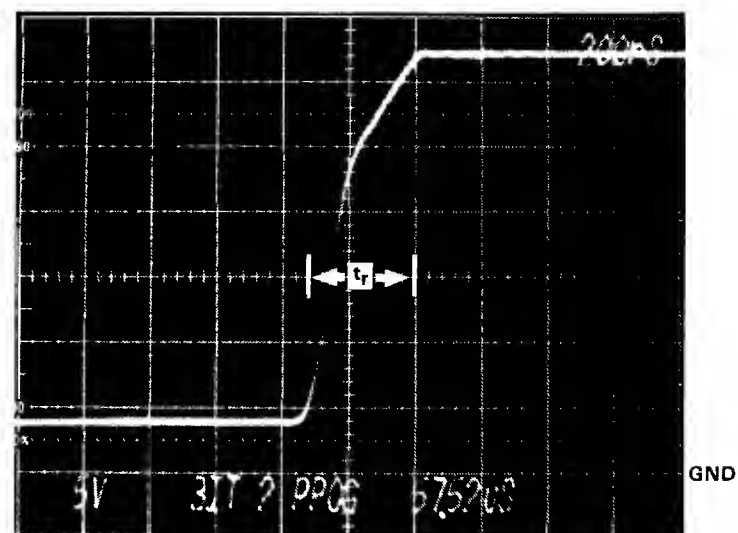
FAMILY CODE 78

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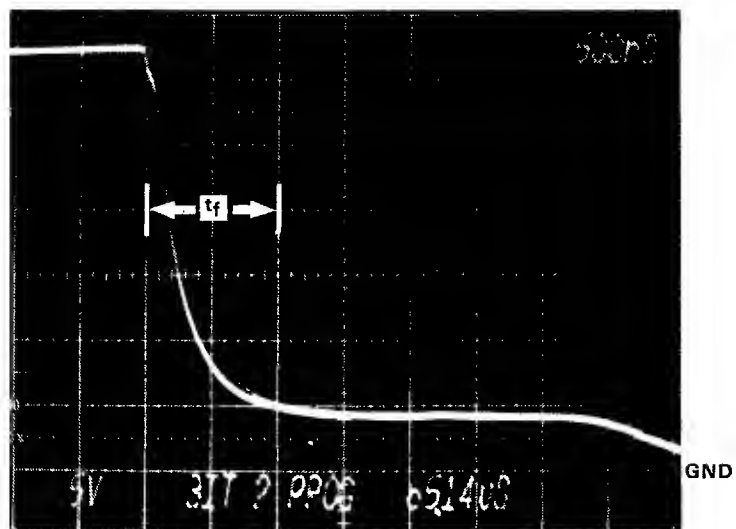
# DATA I/O



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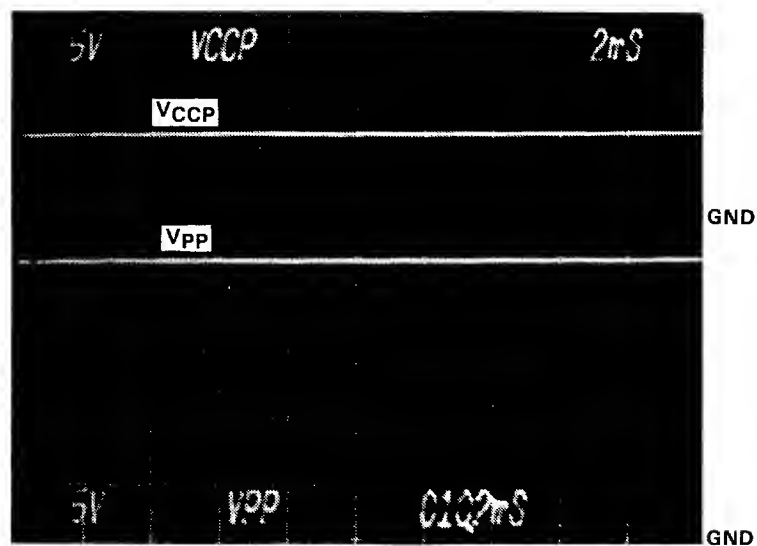
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

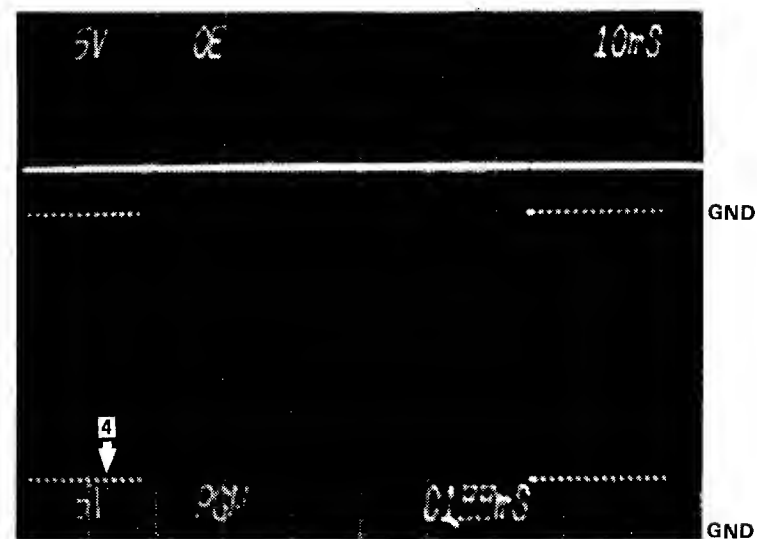
TIMING DIAGRAM

FAMILY CODE 78

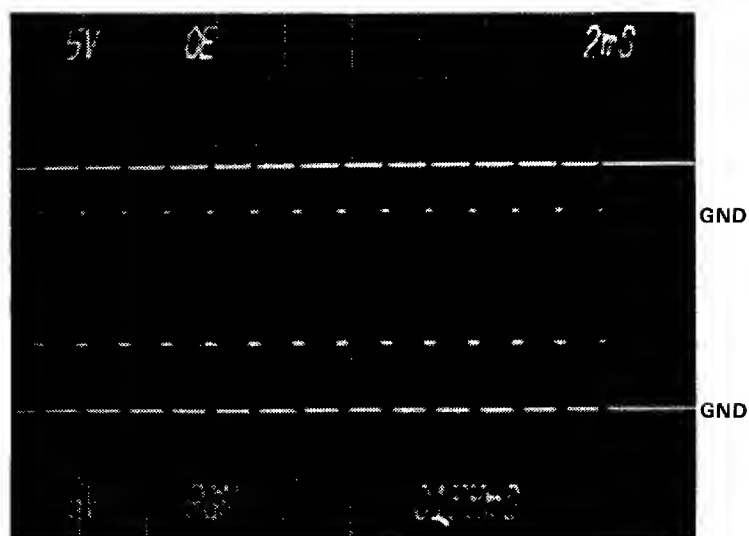
Sheet 2 of 2 **DATA I/O**



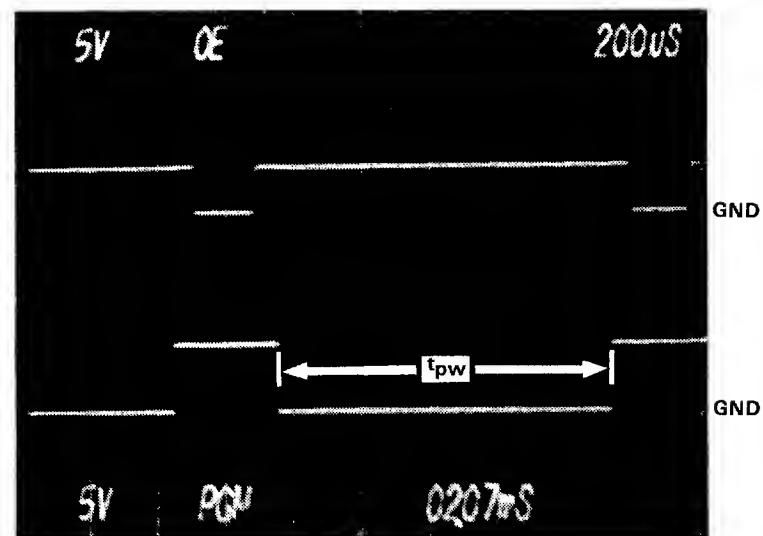
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.75	6.0	6.25	V	
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	20.5	21.0	21.5	V	
	V <sub>PPV</sub>					NA
	t <sub>pw</sub>	0.95	1.0	1.05	ms	
	t <sub>r</sub>					NA
	t <sub>f</sub>					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See note 2
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RSS	5/25/83

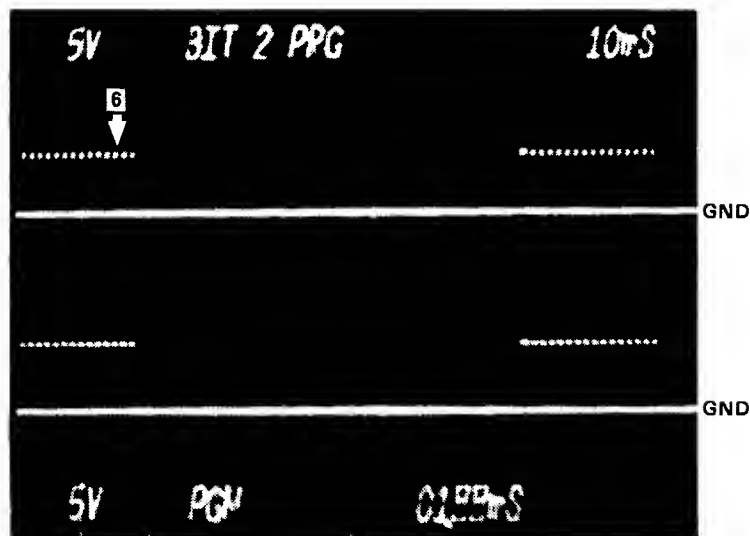
TIMING DIAGRAM

FAMILY CODE 79

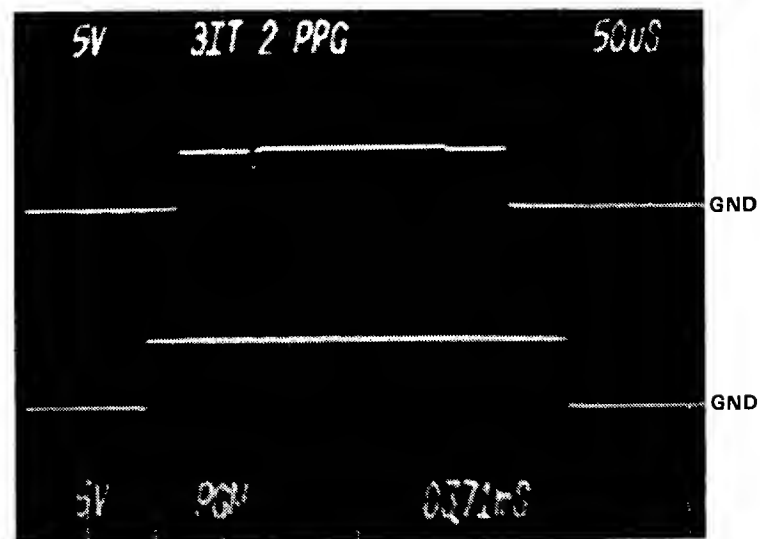
Sheet 1 of 2

# DATA I/O

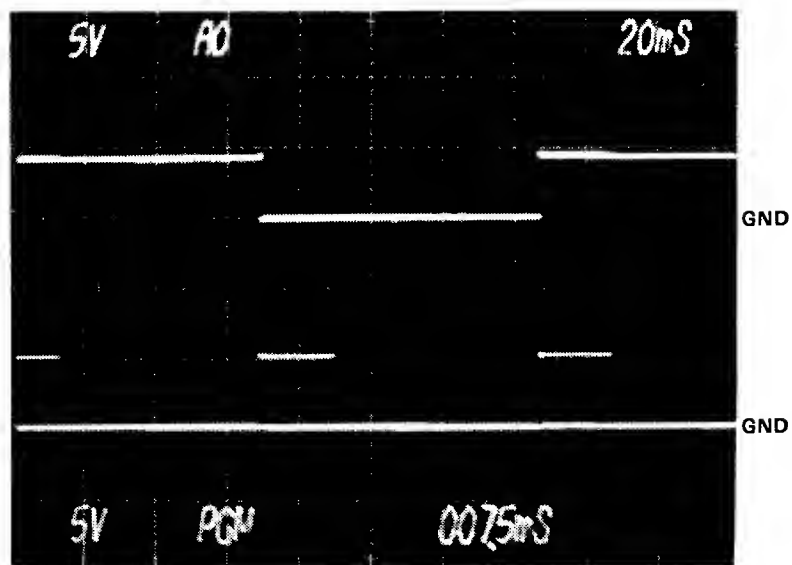




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# REVISIONS

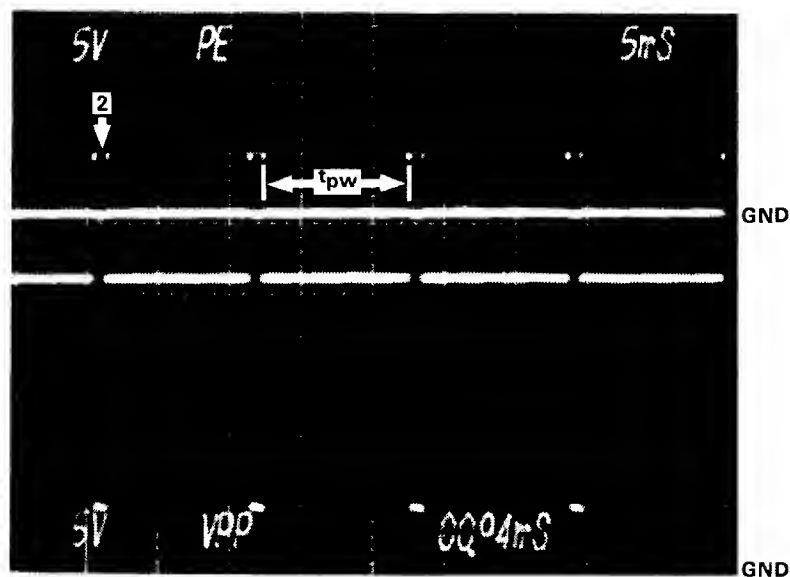
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

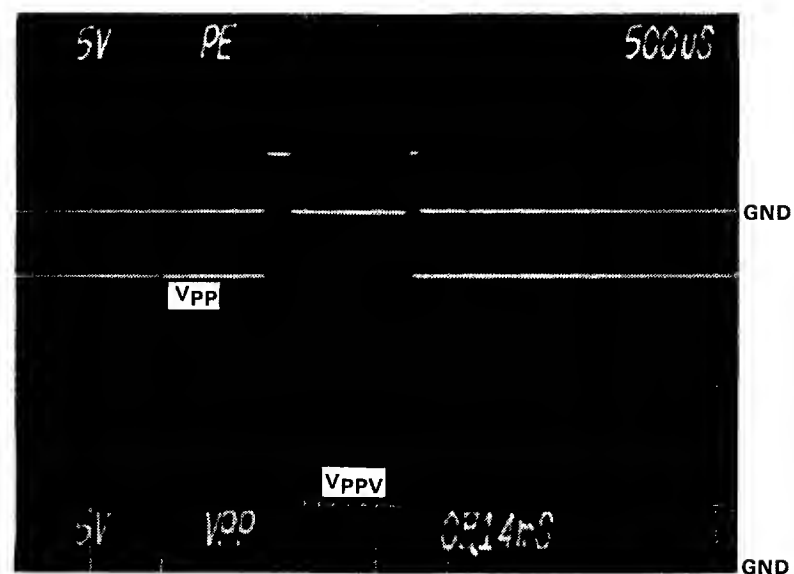
FAMILY CODE 79

Sheet 2 of 2

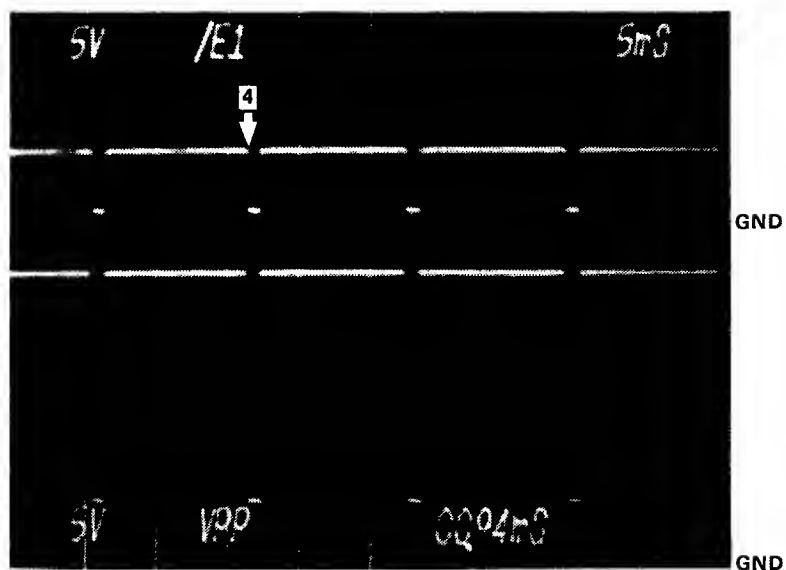
**DATA I/O**



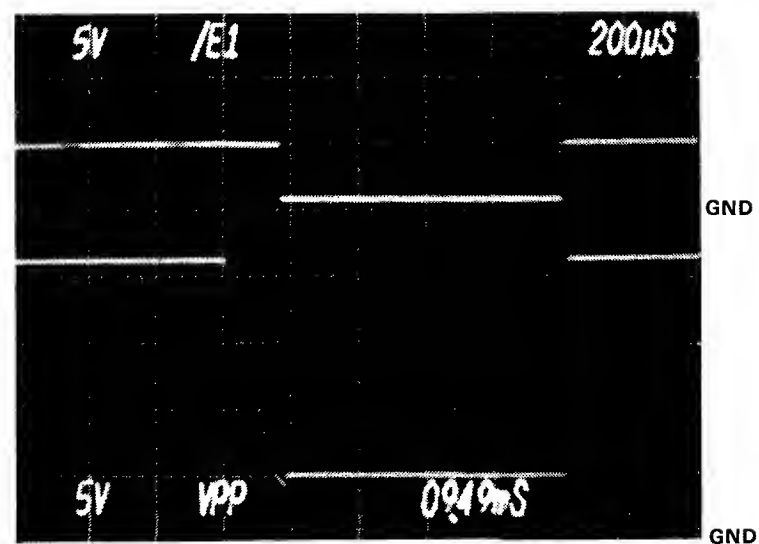
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not Shown NA
	V <sub>OP</sub>					
	V <sub>pp</sub>	20.0	21.0	22.0	V	
	V <sub>PPV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	9.8	10.0	10.2	ms	
	t <sub>r</sub>	1			μs	
	t <sub>f</sub>	1			μs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	
2ND PASS VERIFY	V <sub>CC</sub>	4.9	5.0	5.1	V	702-1775/TP18 702-1775/TP15 702-1775/TP14
	V <sub>REF</sub>	1.4	1.5	1.6	V	
	High Load	0.0	0.0	0.5	V	
	Low Load	13.1	13.5	13.9	V	

## NOTES

1. Load RAM with \$FE.
2. Photos 13 thru 18 are erase waveforms.

## REVISIONS

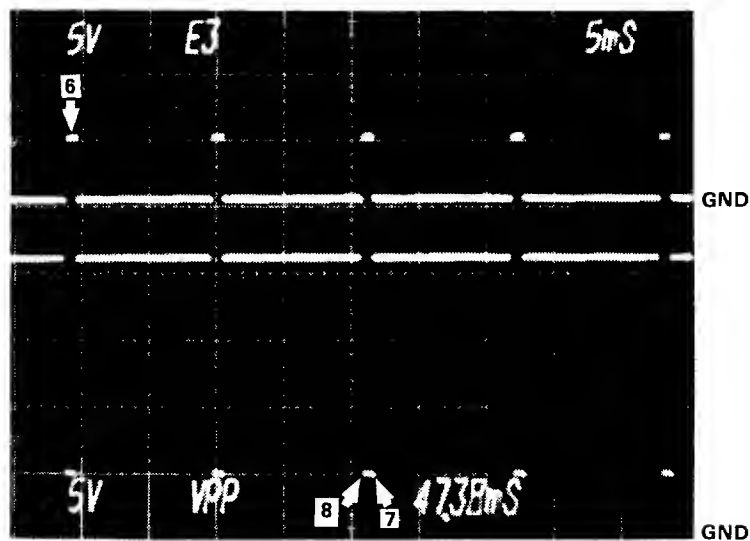
LTR	DESCRIPTION	P.E.	DATE
A	Release	RJJ	5/25/03

**TIMING DIAGRAM**

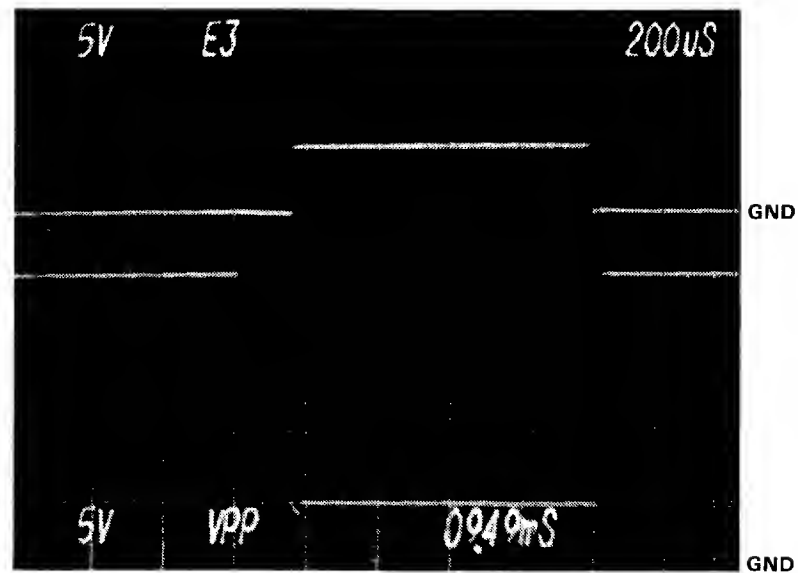
**FAMILY CODE 81**

Sheet 1 of 5

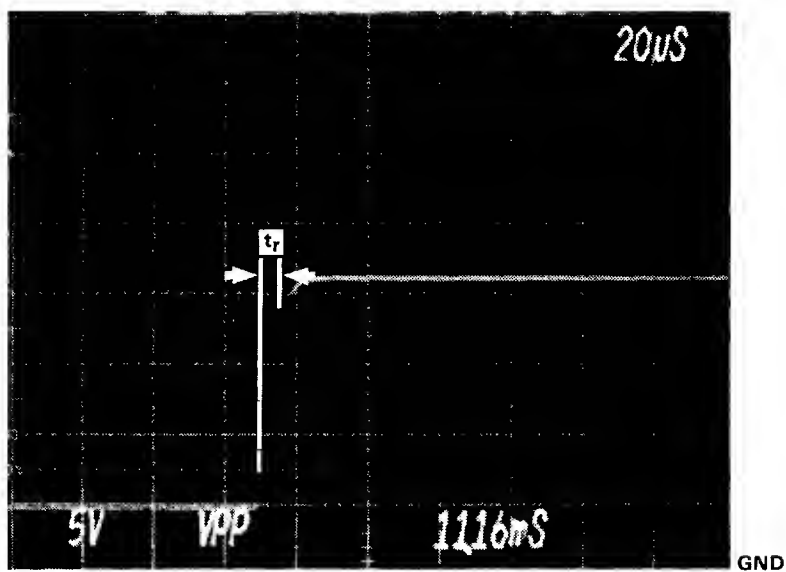
# DATA I/O



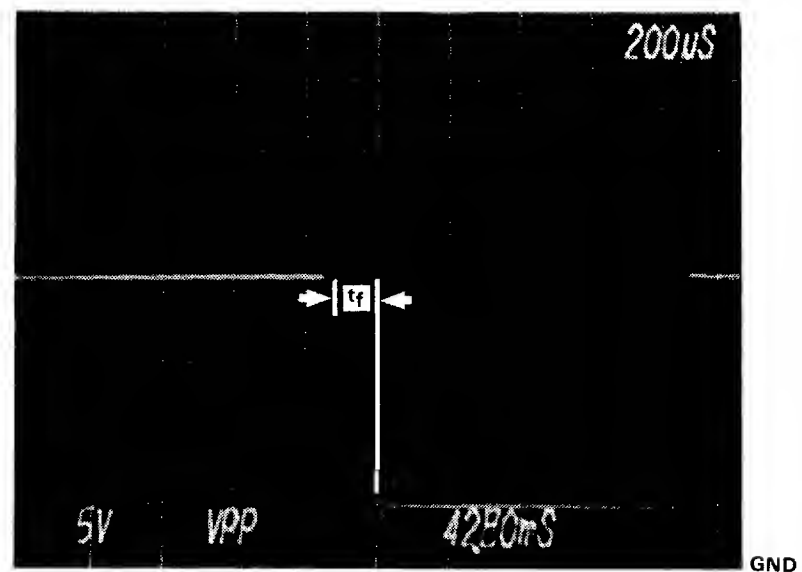
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# REVISIONS

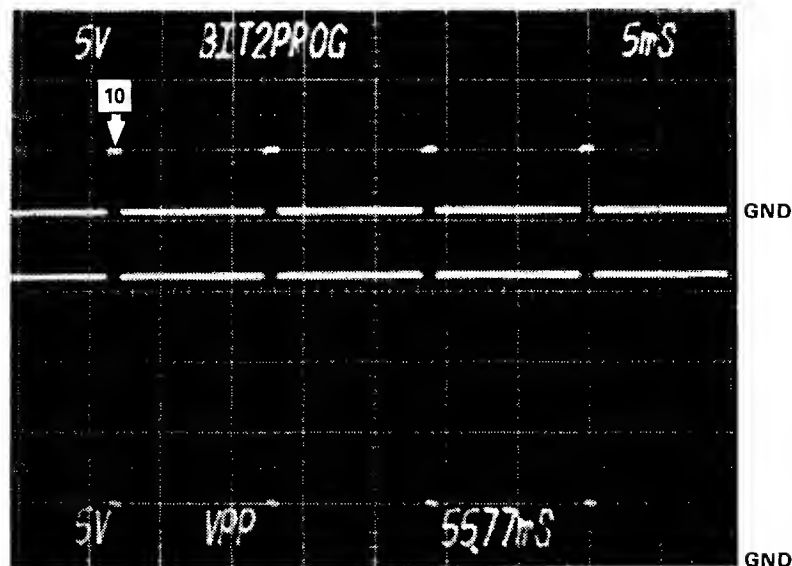
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

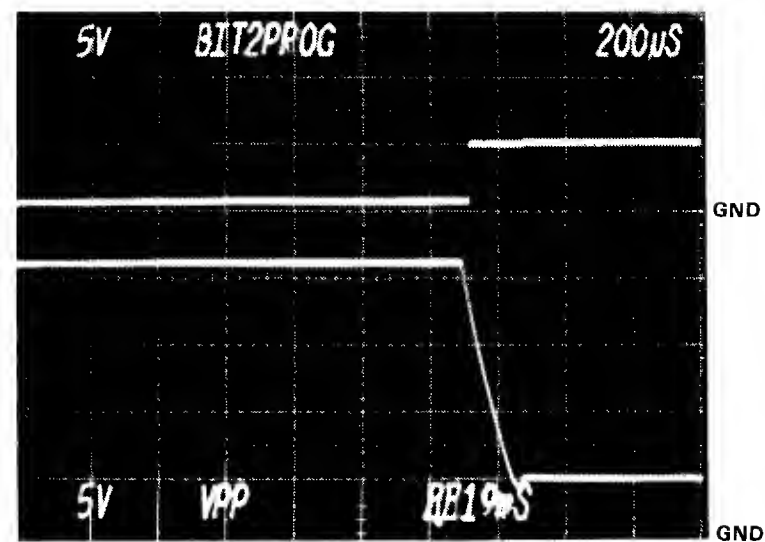
FAMILY CODE 81

Sheet 2 of 5

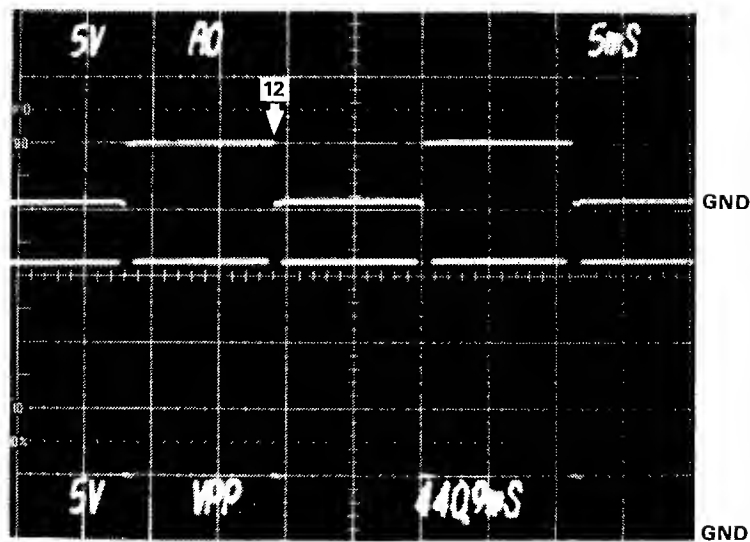
**DATA I/O**



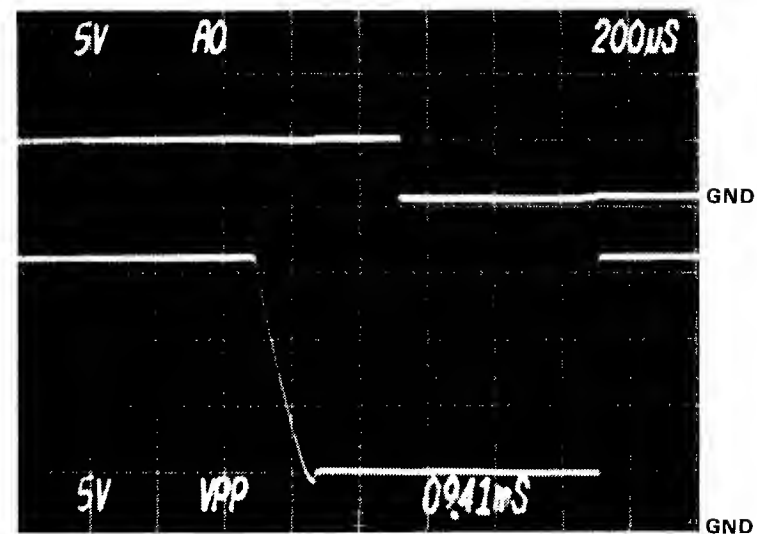
9



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11



12

# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

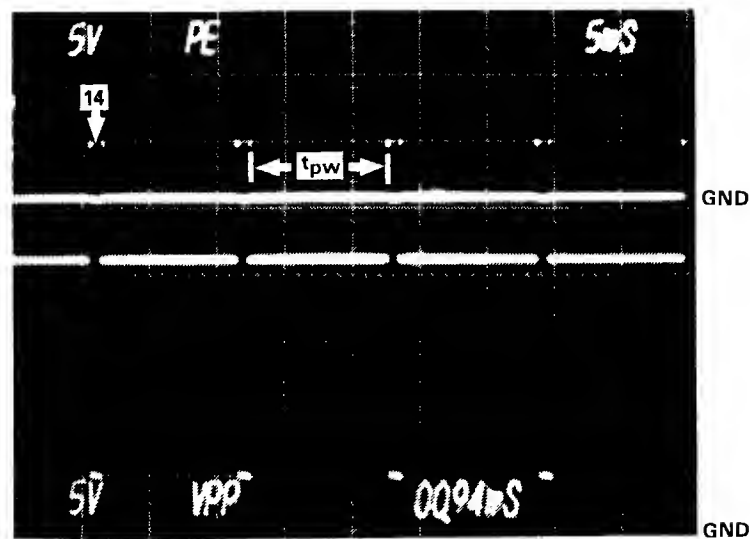
TIMING DIAGRAM

FAMILY CODE 81

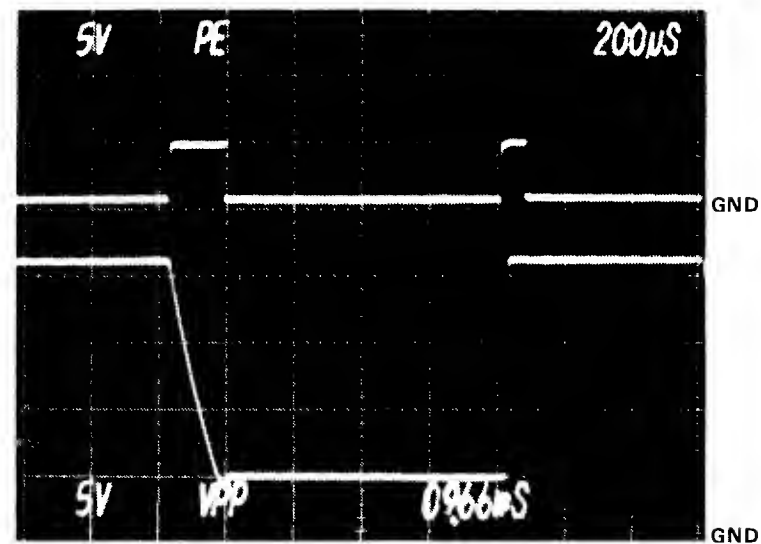
Sheet 3 of 5

**DATA I/O**

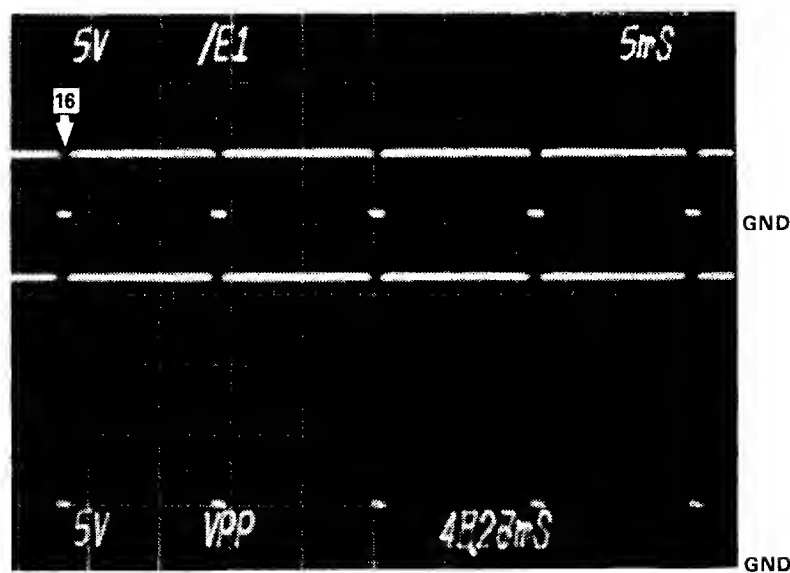




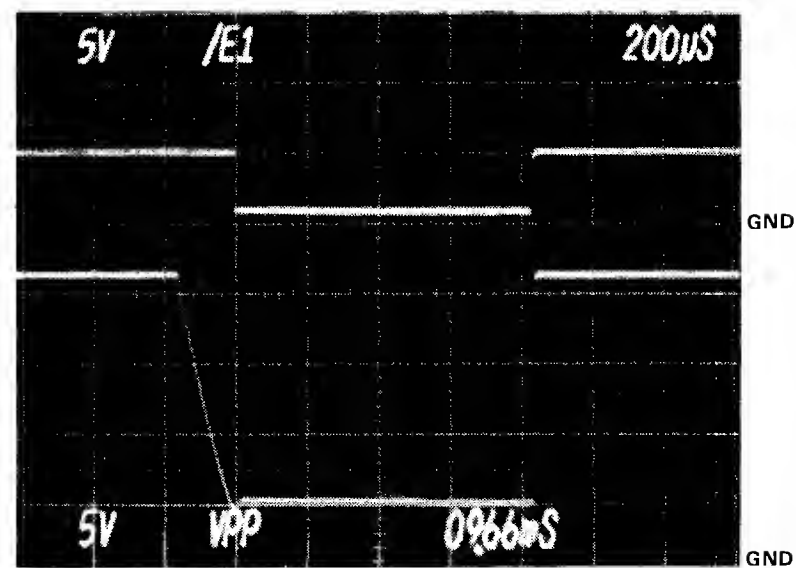
13



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REVISIONS

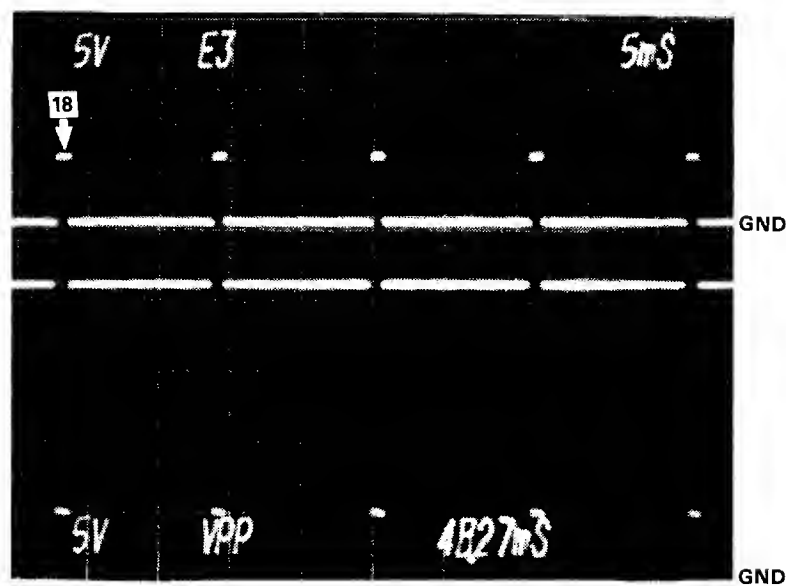
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

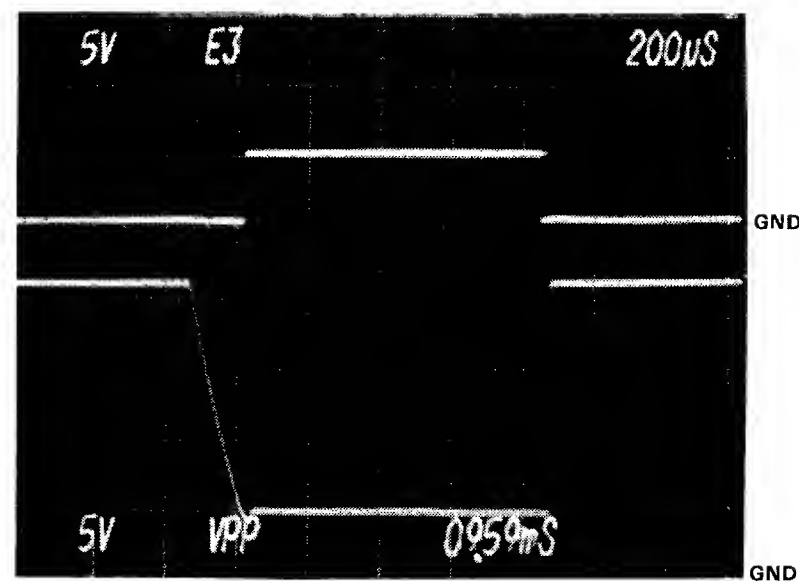
FAMILY CODE 81

Sheet 4 of 5

**DATA I/O**



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18

# REVISIONS

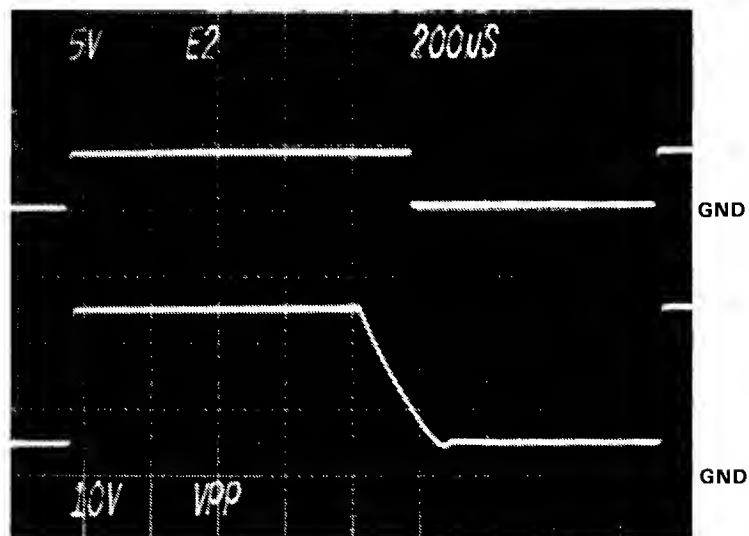
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

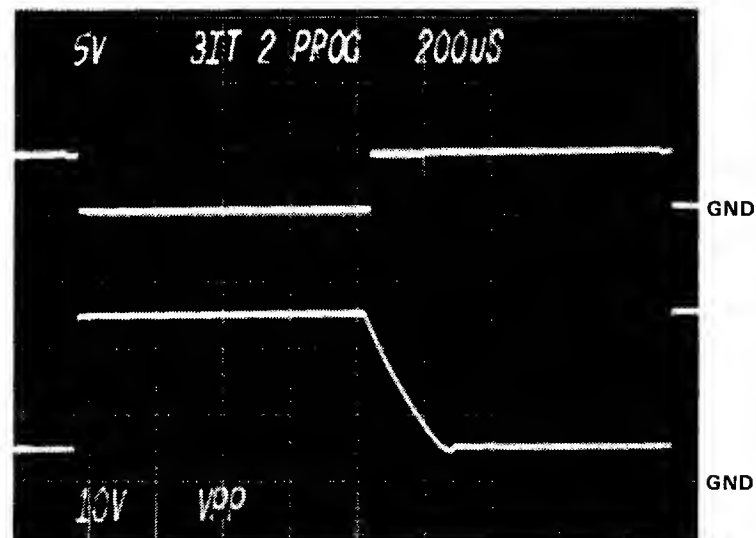
FAMILY CODE 81

Sheet 5 of 5

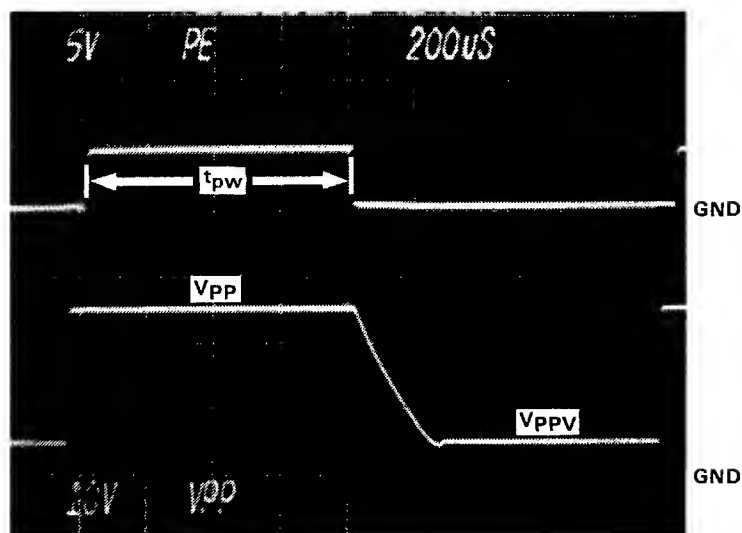
**DATA I/O**



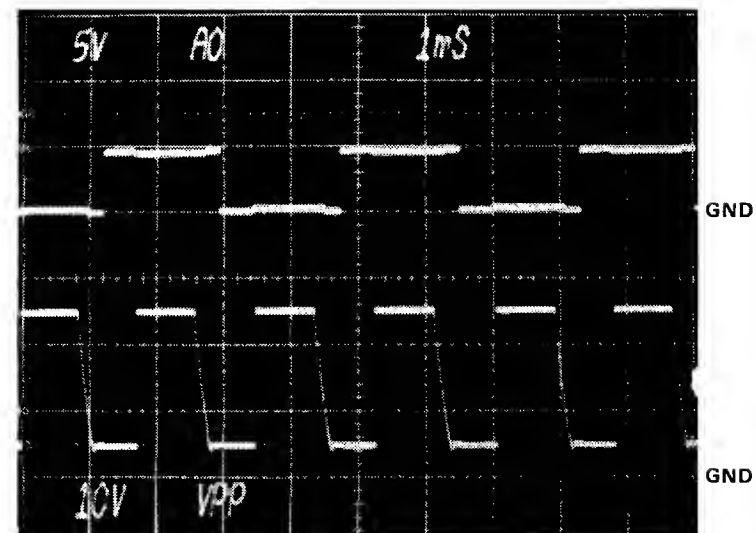
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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not shown
	V <sub>OP</sub>					NA
	V <sub>pp</sub>	24.0	25.0	26.0	V	
	V <sub>ppV</sub>	4.75	5.0	5.25	V	
	t <sub>pw</sub>	800			μs	
	t <sub>r</sub>	5			ns	
	t <sub>ep</sub>	1			sec	
	t <sub>f</sub>	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.

## REVISIONS

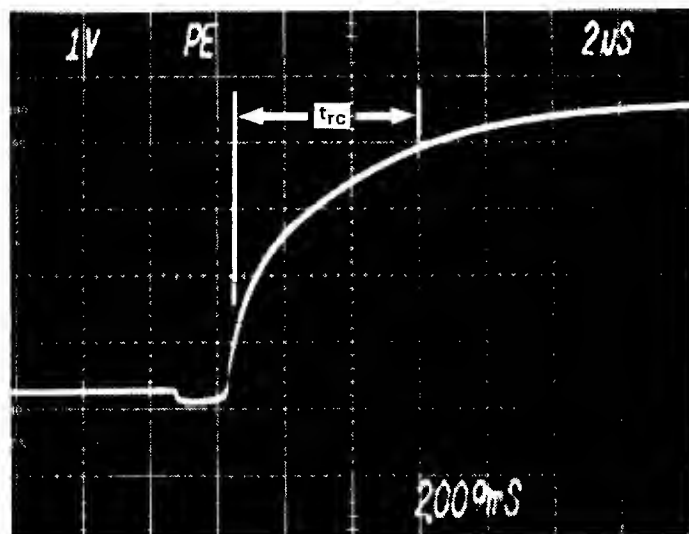
LTR	DESCRIPTION	P.E.	DATE
A	Release	RJS	5/25/83

TIMING DIAGRAM

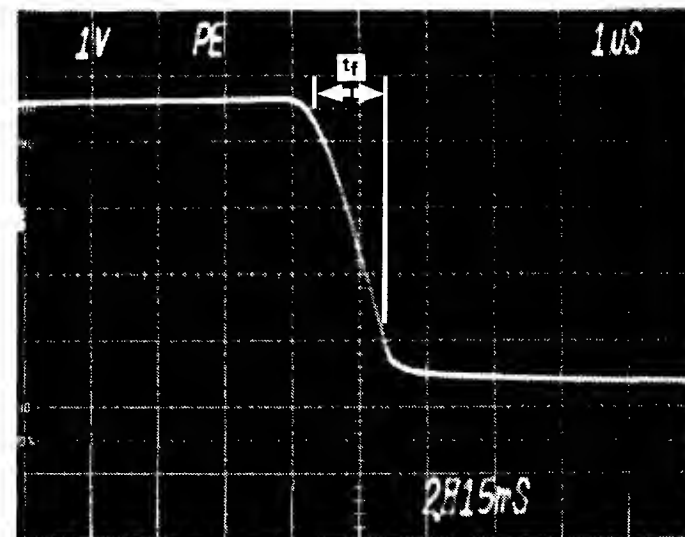
FAMILY CODE 83

Sheet 1 of 2

**DATA I/O**



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# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

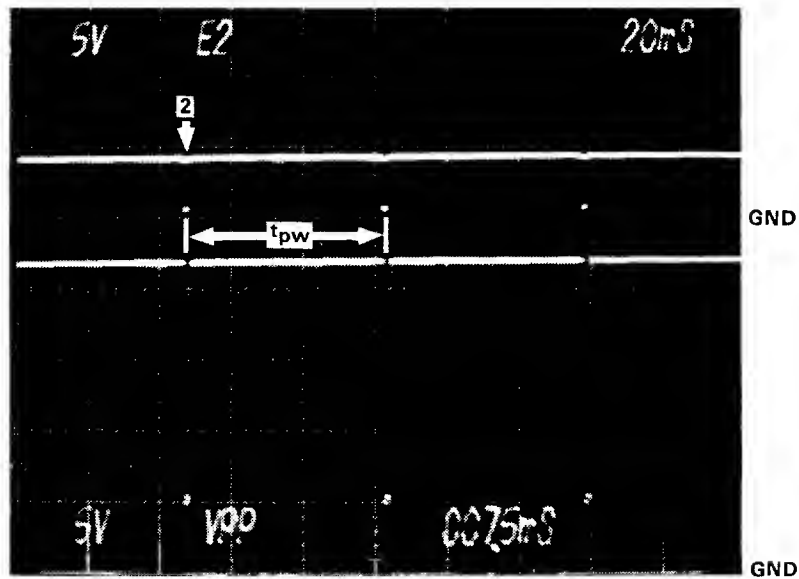
TIMING DIAGRAM

FAMILY CODE 83

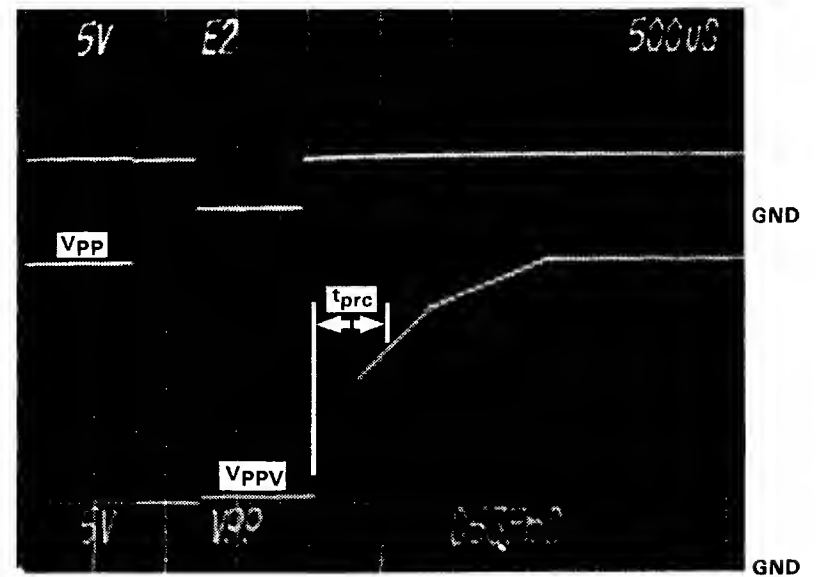
Sheet 2 of 2

**DATA I/O**

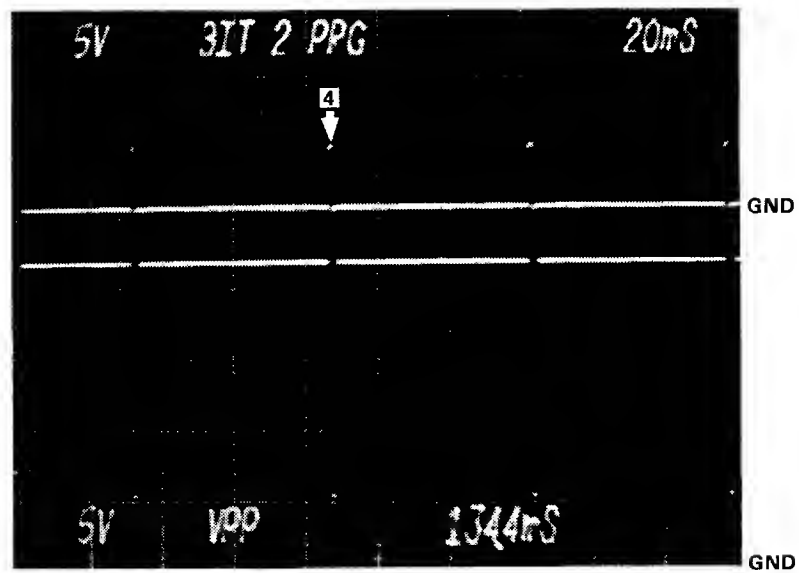




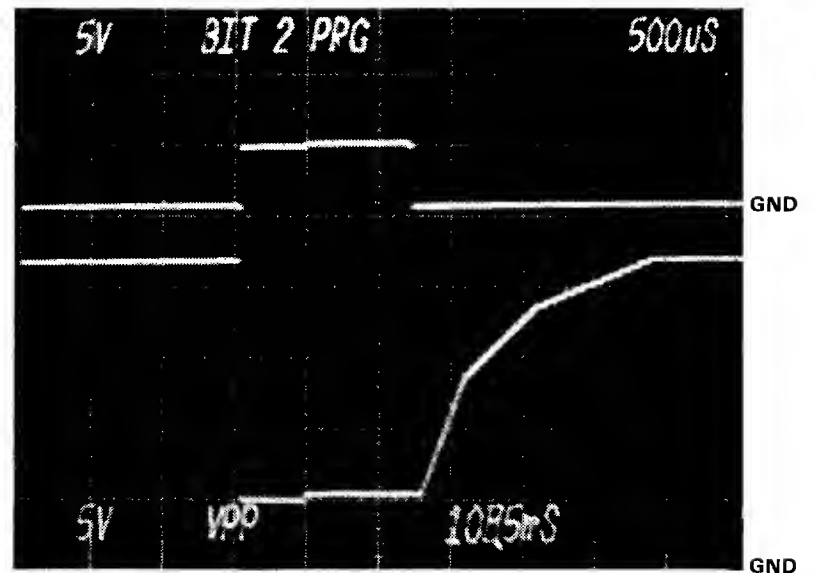
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# FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not shown
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	20.0	21.0	22.0	V	
	V <sub>PPV</sub>	4.0	5.0	6.0	V	
	V <sub>EE</sub>	9.0		15.0	V	
	t <sub>pw</sub>	50		70	ms	
	t <sub>prc</sub>	450	600	700	μs	See note 2
	t <sub>f</sub>			100	μs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	0.4	0.5	0.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	2.3	2.4	2.5	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

# NOTES

1. Load RAM with \$FE.
2. TPRC is measured from 6V to 15.5V.
3. Photos 8 and 9 are erase waveforms.

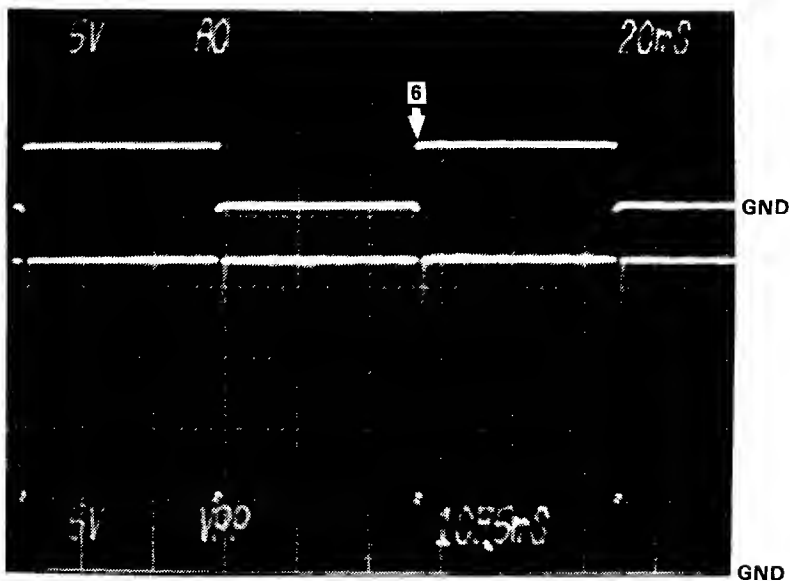
# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RJJ	5/25/83

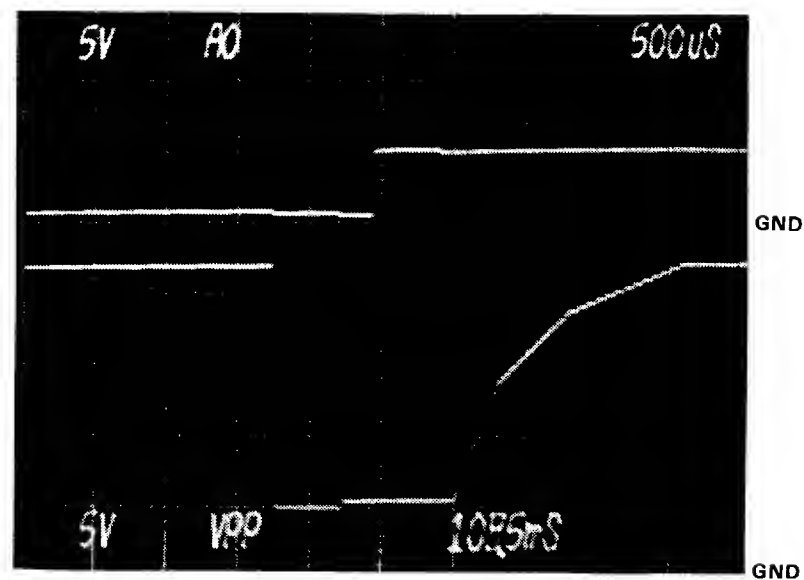
TIMING DIAGRAM

FAMILY CODE 85

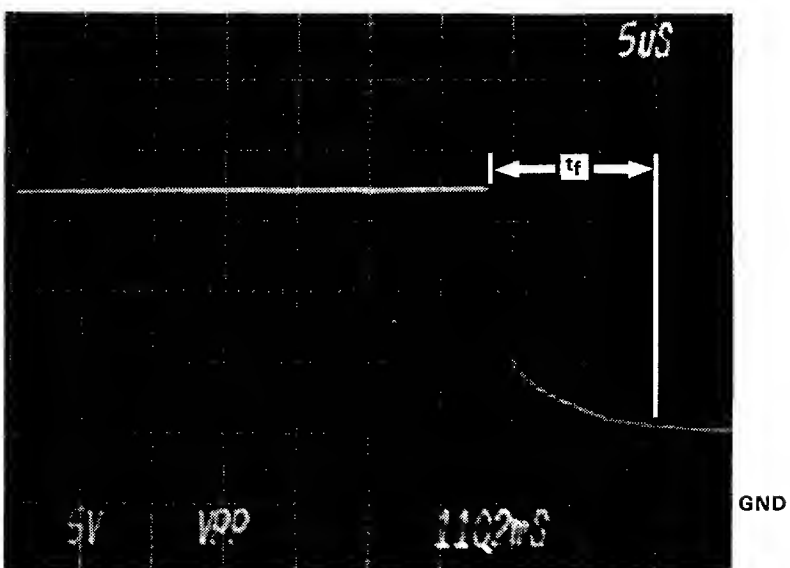
Sheet 1 of 3 **DATA I/O**



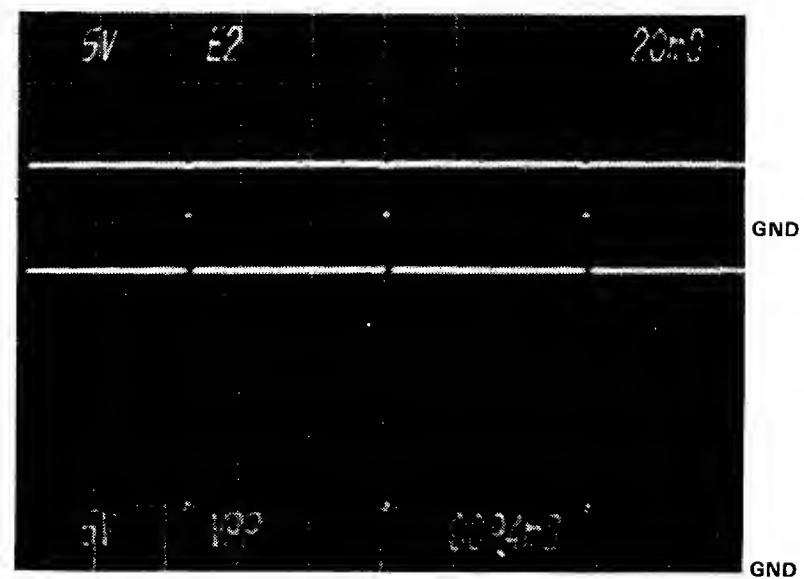
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# REVISIONS

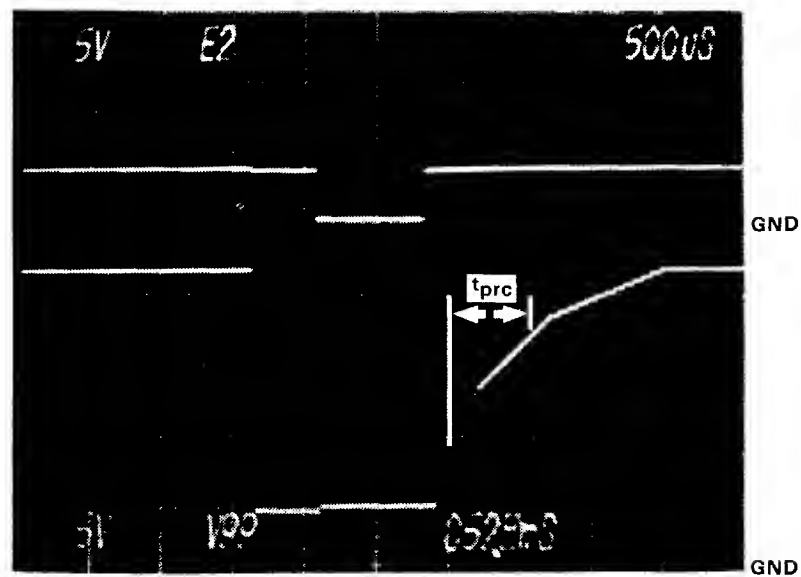
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

FAMILY CODE 85

Sheet 2 of 3

**DATA I/O**



# REVISIONS

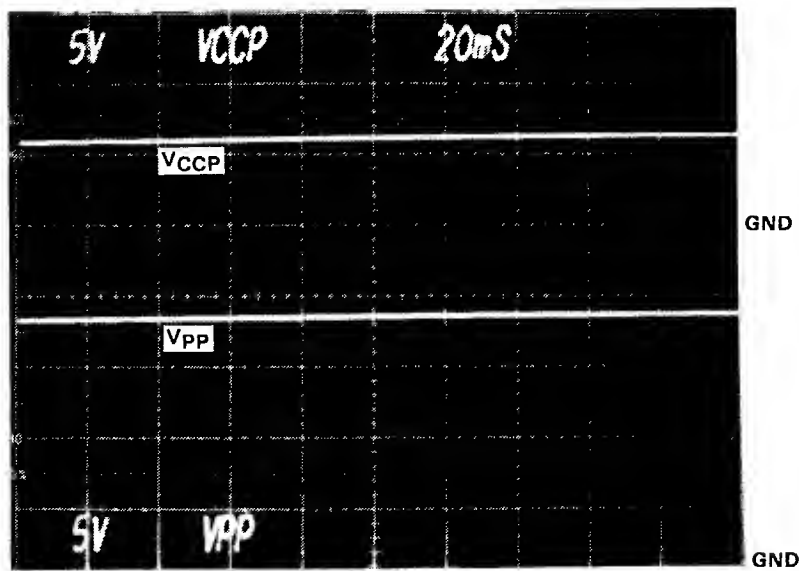
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

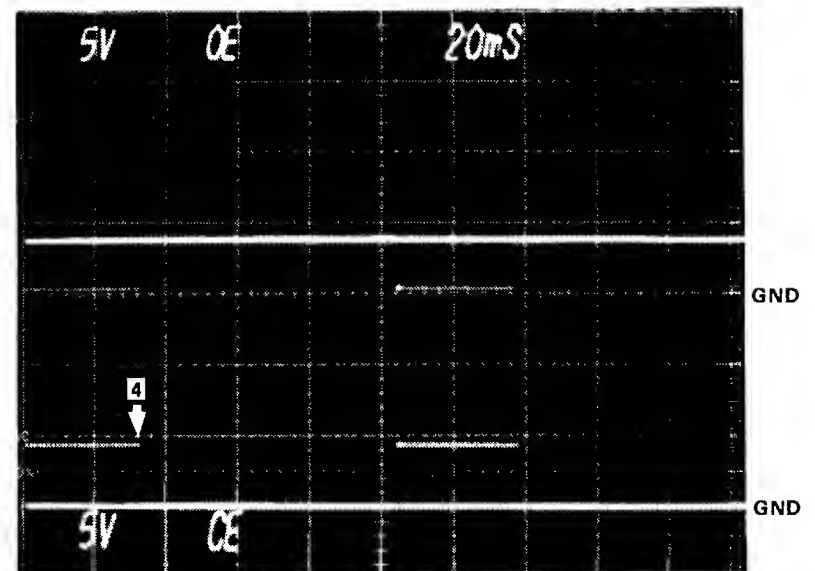
FAMILY CODE 85

Sheet 3 of 3

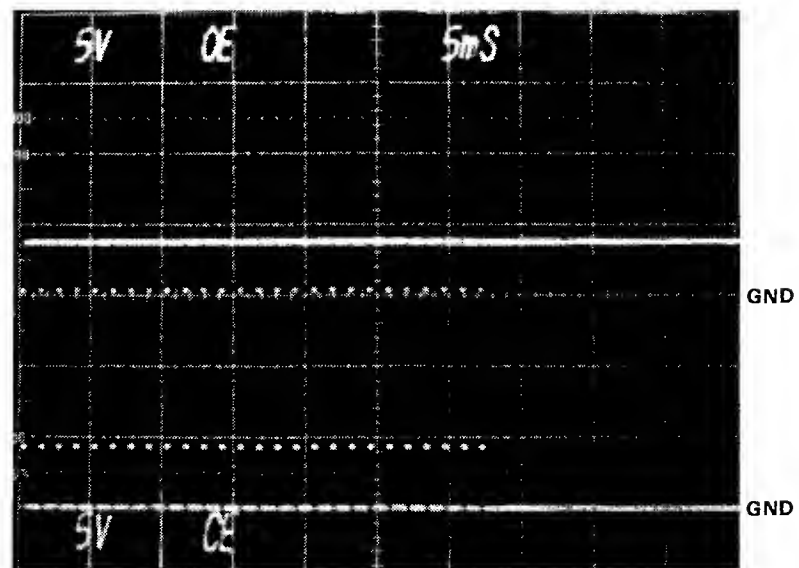
**DATA I/O**



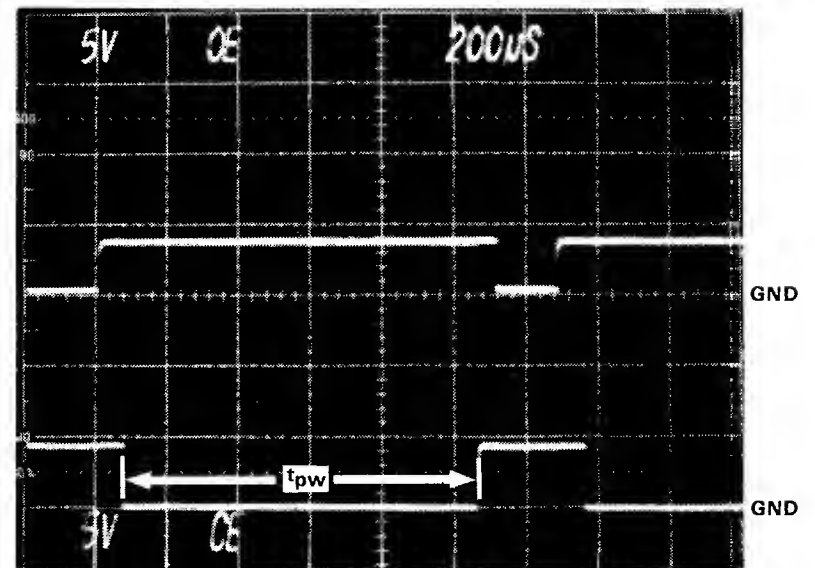
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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.75	6.0	6.25	V	
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	12.20	12.50	12.80	V	
	V <sub>PPV</sub>					NA
	t <sub>pw</sub>	0.95	1.0	1.05	ms	See note 3
	t <sub>r</sub>					NA
	t <sub>f</sub>					NA
	Reject		25		Pulses	
	Overprogram		1		Pulses	See note 2
1ST PASS	V <sub>CC</sub>	4.7	4.8	4.9	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.0	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	5.6	5.7	5.8	V	
VERIFY	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.0	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.
2. The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 3ms.
3. For pinout 32, CE is as shown. For pinouts 33 and 51, CE waveform in photos represents PGM line.

## REVISIONS

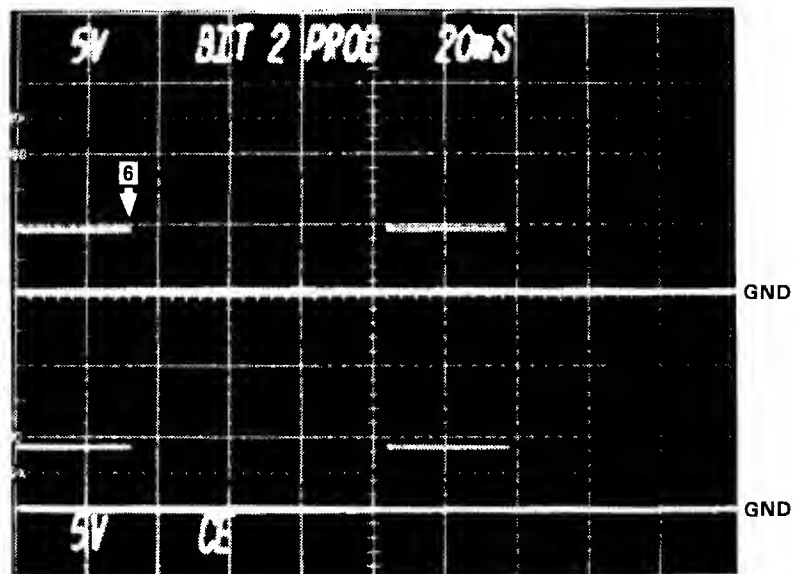
LTR	DESCRIPTION	P.E.	DATE
A	Release	RMS	5/25/03

TIMING DIAGRAM

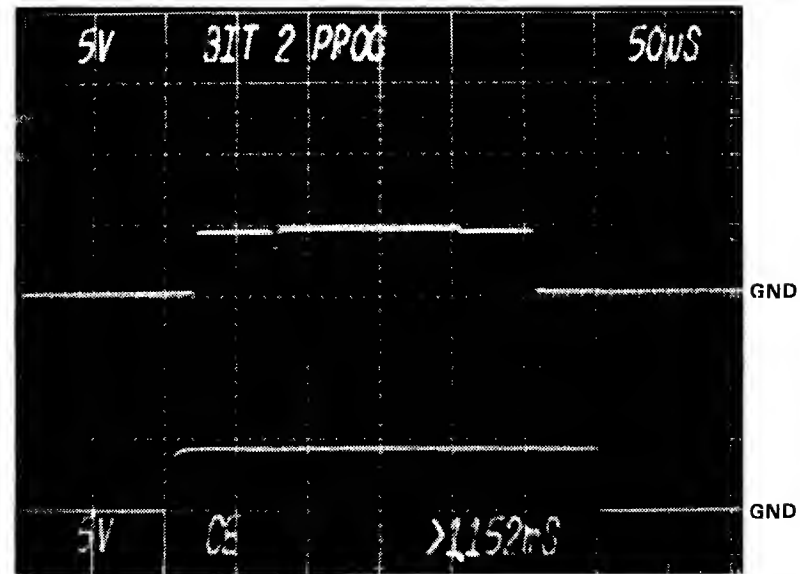
FAMILY CODE 93

Sheet 1 of 2 **DATA I/O**

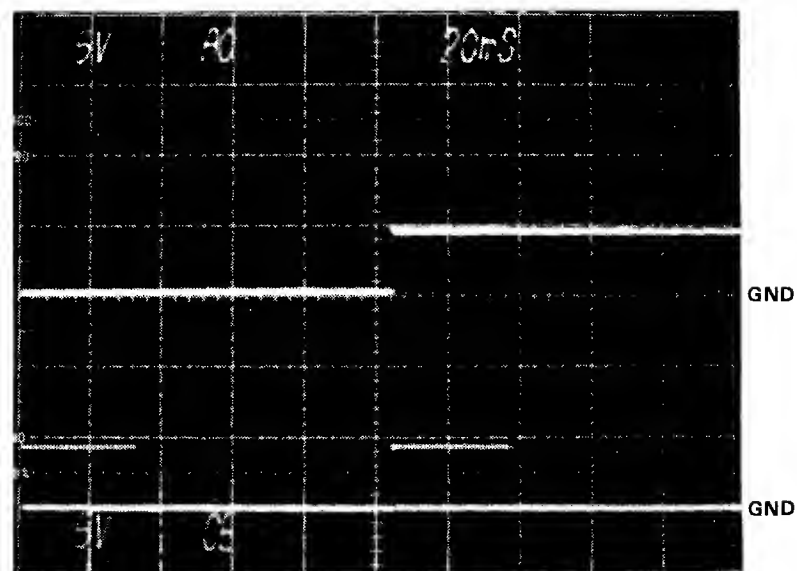




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REVISIONS

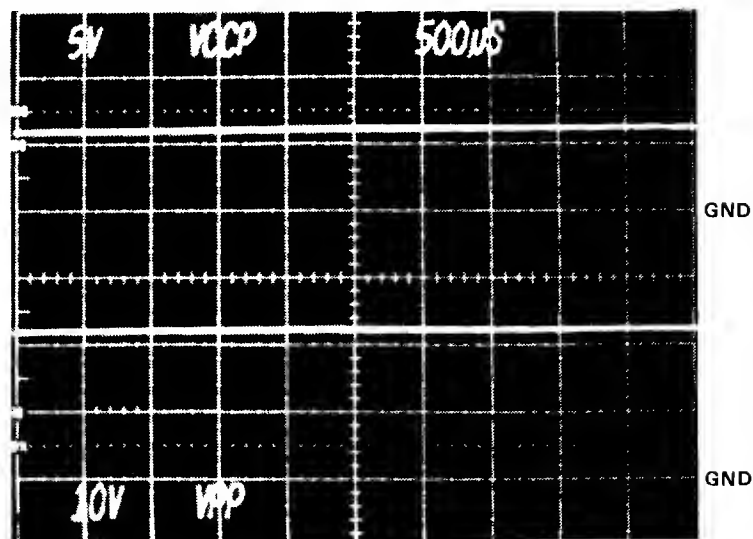
LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

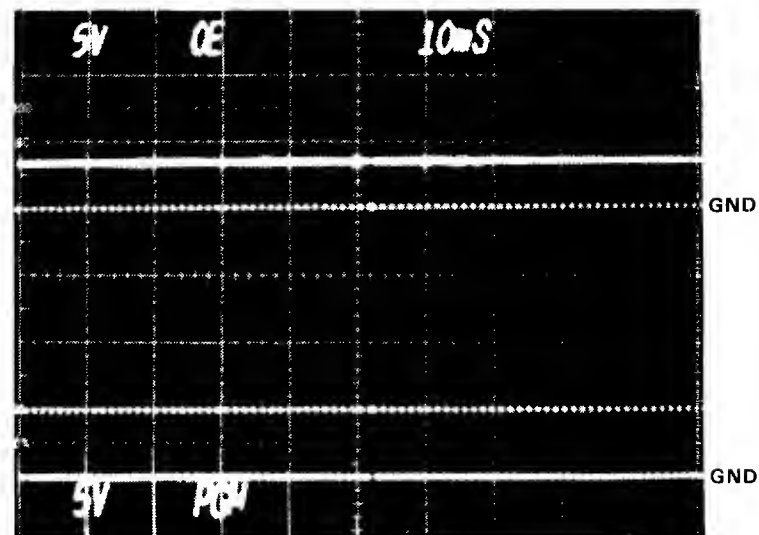
FAMILY CODE 93

**DATA I/O**

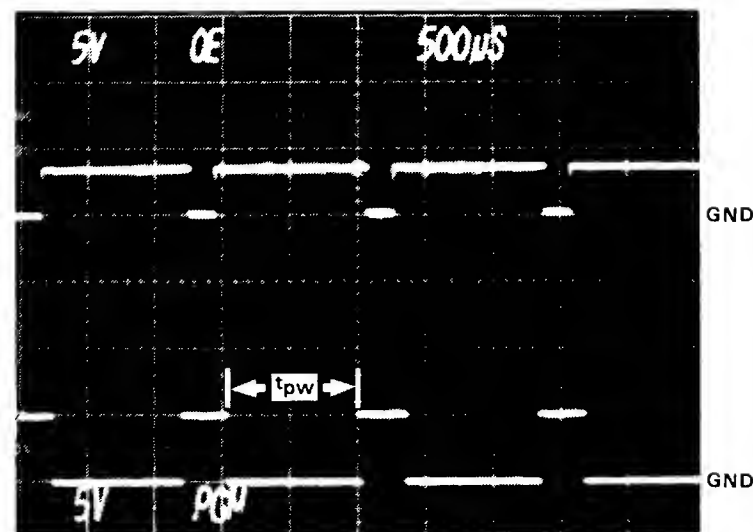
Sheet 2 of 2



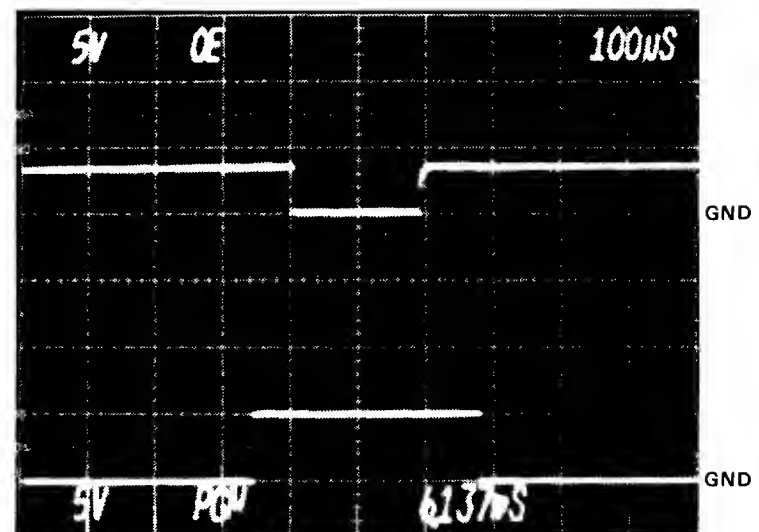
1



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## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	5.75	6.0	6.25	V	
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	21.0	21.5	22.0	V	
	V <sub>PPV</sub>					NA
	t <sub>pw</sub>	0.95	1.0	1.05	ms	
	t <sub>r</sub>					NA
	t <sub>f</sub>					NA
	Reject		40		Pulses	
	Overprogram		1		Pulses	4ms
1ST PASS VERIFY	V <sub>CC</sub>	4.7	4.8	4.9	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.0	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS VERIFY	V <sub>CC</sub>	5.5	5.6	5.7	V	
	V <sub>REF</sub>	1.4	1.5	1.6	V	702-1775/TP18
	High Load	0.0	0.0	0.0	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.

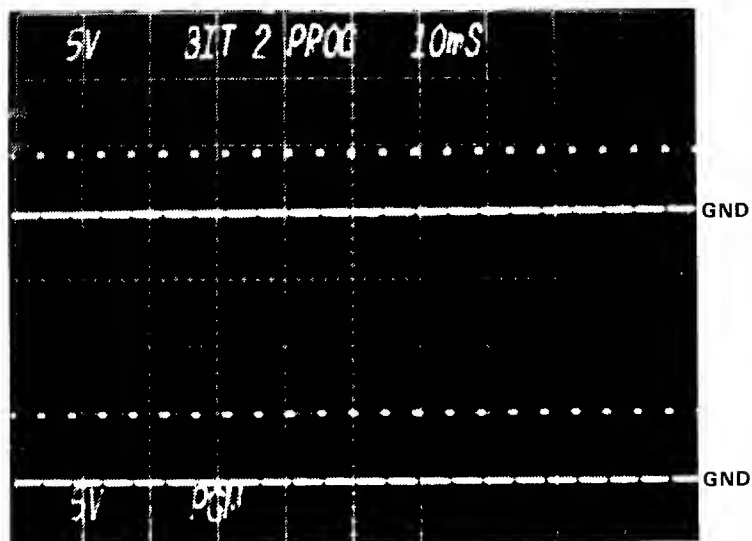
## REVISIONS

LTR	DESCRIPTION	P. E.	DATE
A	Release	R22	5/25/03

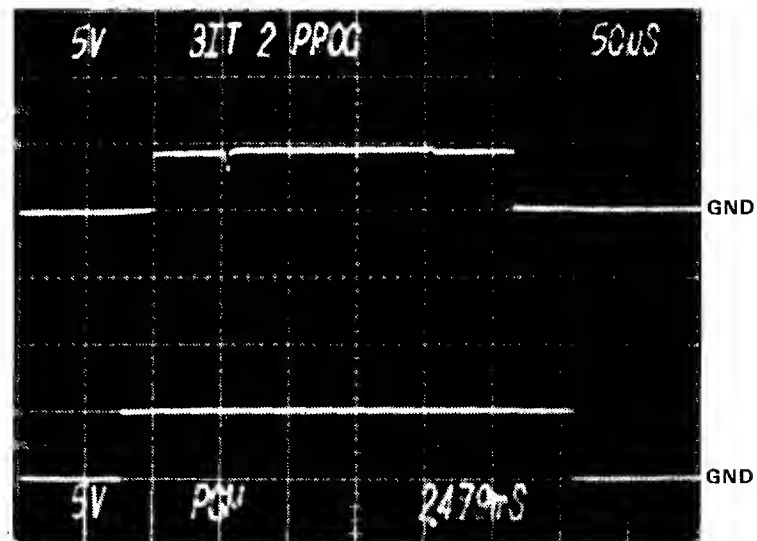
TIMING DIAGRAM

FAMILY CODE AF

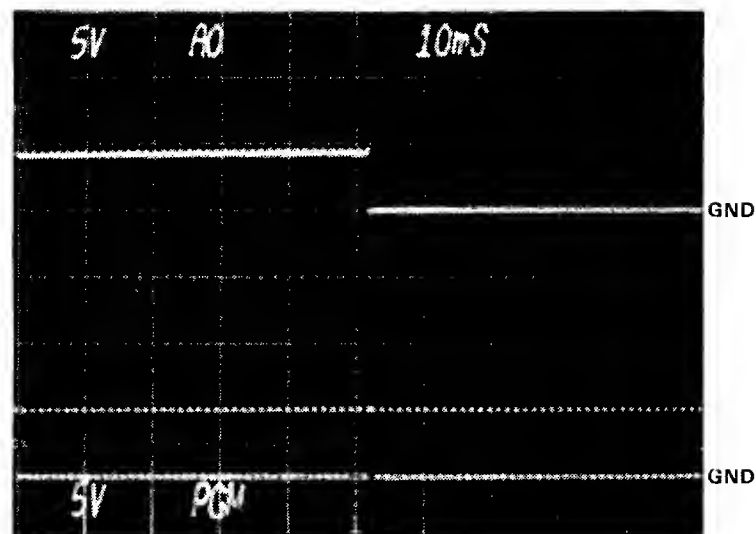
Sheet 1 of 2 **DATA I/O**



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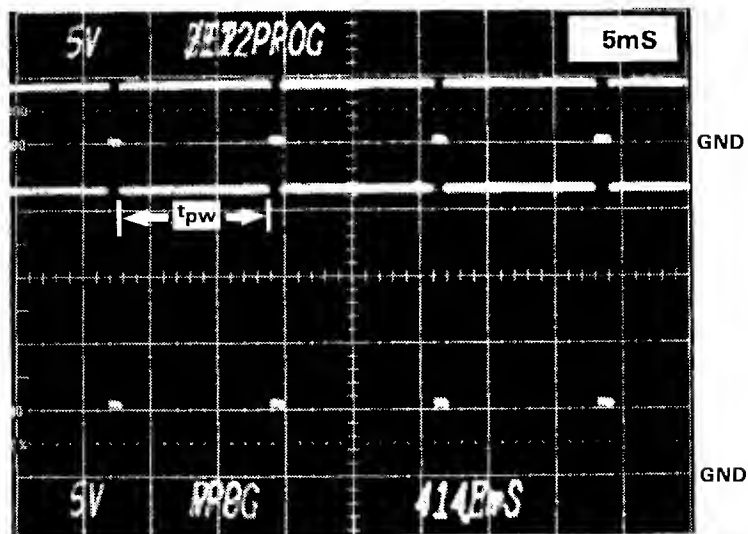
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

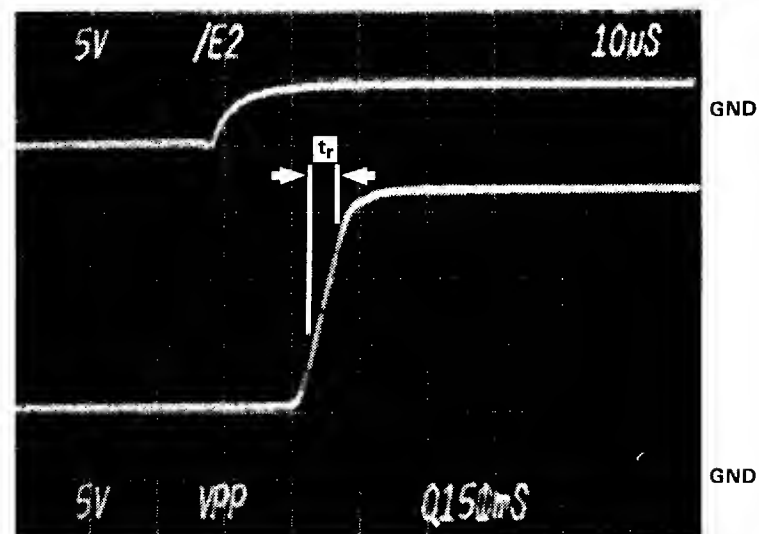
TIMING DIAGRAM

FAMILY CODE AF

Sheet 2 of 2 **DATA I/O**



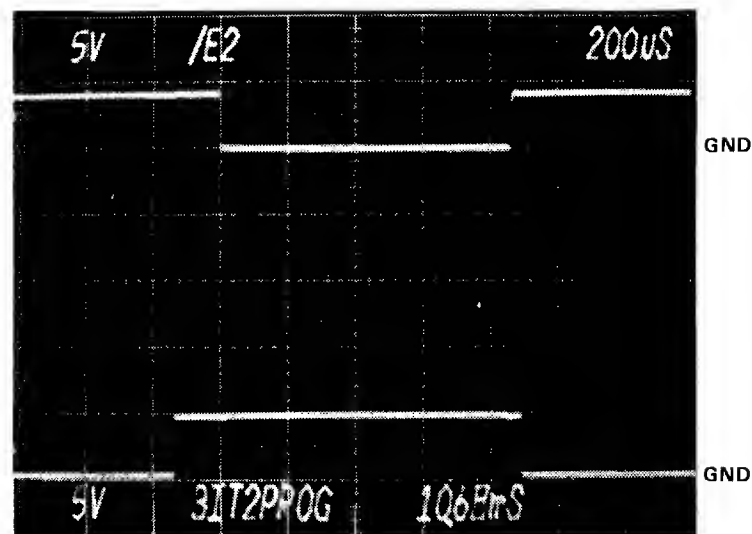
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2



3



4

## FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V <sub>CCP</sub>	4.75	5.0	5.25	V	Not shown
	V <sub>OP</sub>					NA
	V <sub>PP</sub>	20.5	21.0	21.5	V	
	V <sub>PPV</sub>	4.5	5.0	5.5	V	
	V <sub>OE</sub>	9.0	12.0	15.0	V	
	t <sub>pw</sub>	9.0	10.0	15.0	ms	
	t <sub>r</sub>		6		μs	
	t <sub>f</sub>		100		μs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	0.4	0.5	0.6	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14
2ND PASS	V <sub>CC</sub>	4.9	5.0	5.1	V	
VERIFY	V <sub>REF</sub>	2.3	2.4	2.5	V	702-1775/TP18
	High Load	0.0	0.0	0.5	V	702-1775/TP15
	Low Load	13.1	13.5	13.9	V	702-1775/TP14

## NOTES

1. Load RAM with \$FE.

## REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	RSS	5/25/03

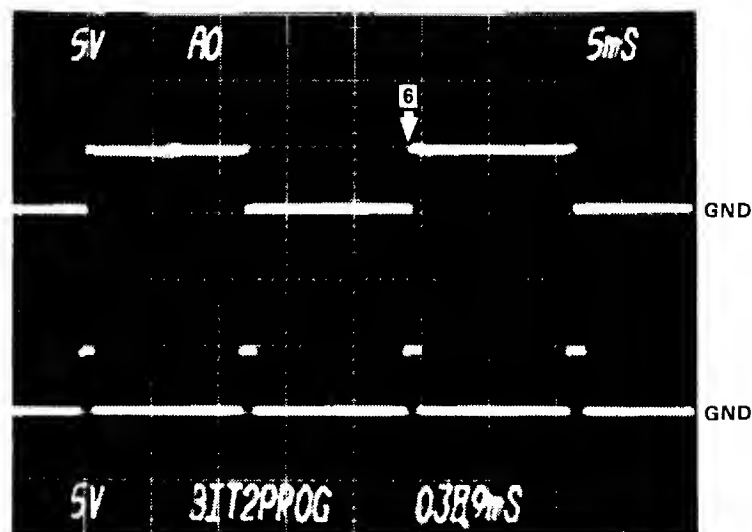
TIMING DIAGRAM

FAMILY CODE B3

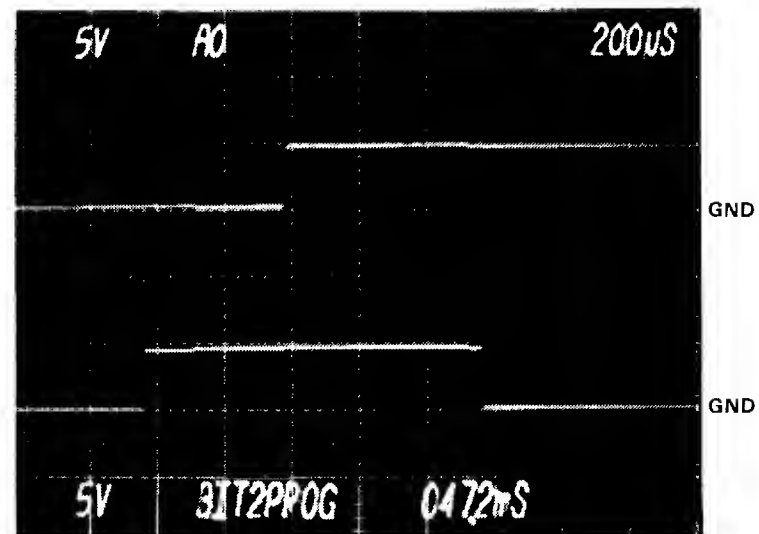
Sheet 1 of 3

# DATA I/O

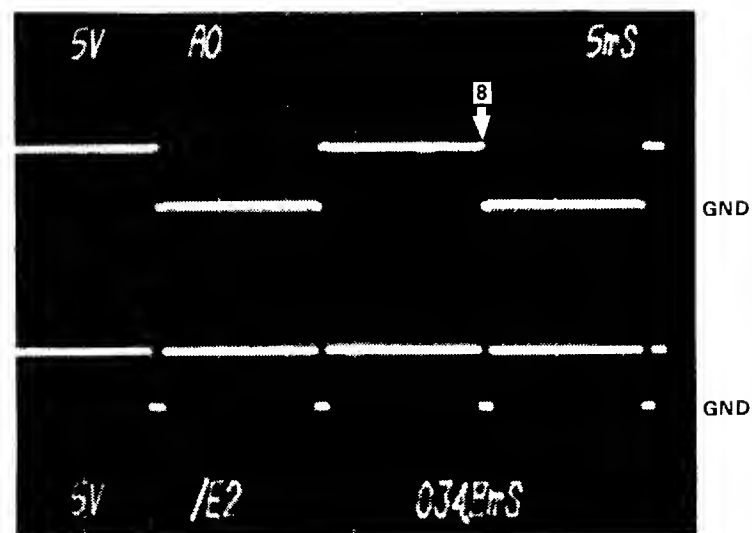




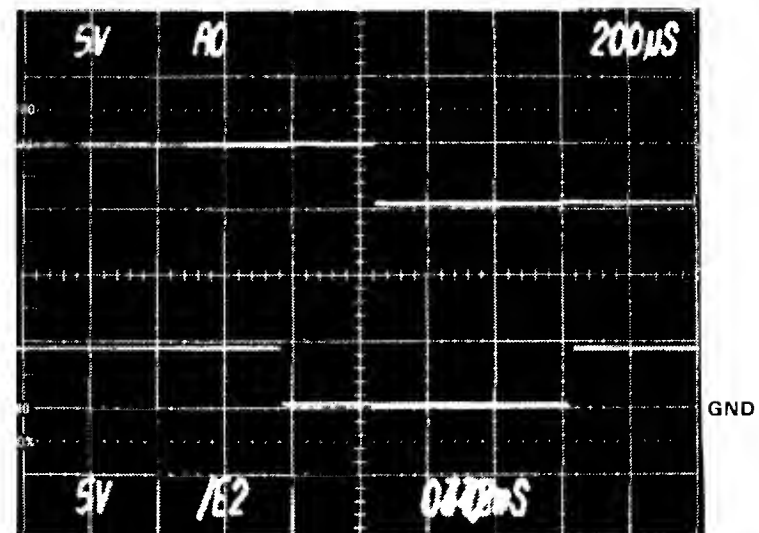
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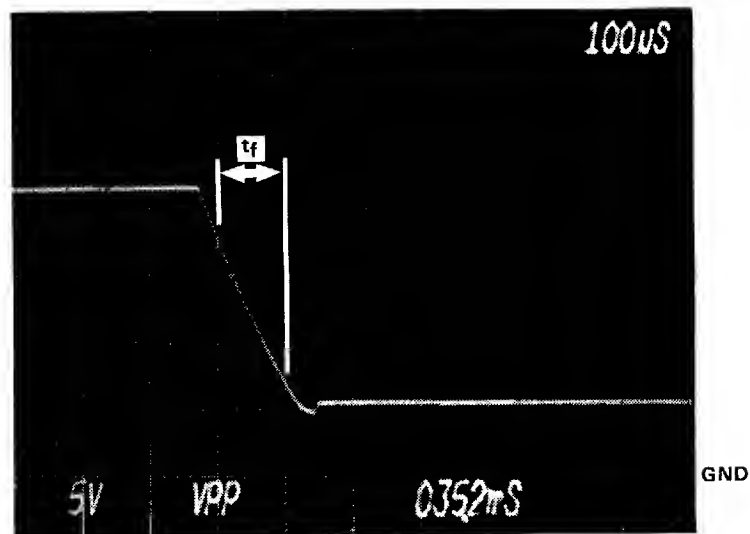
REVISIONS

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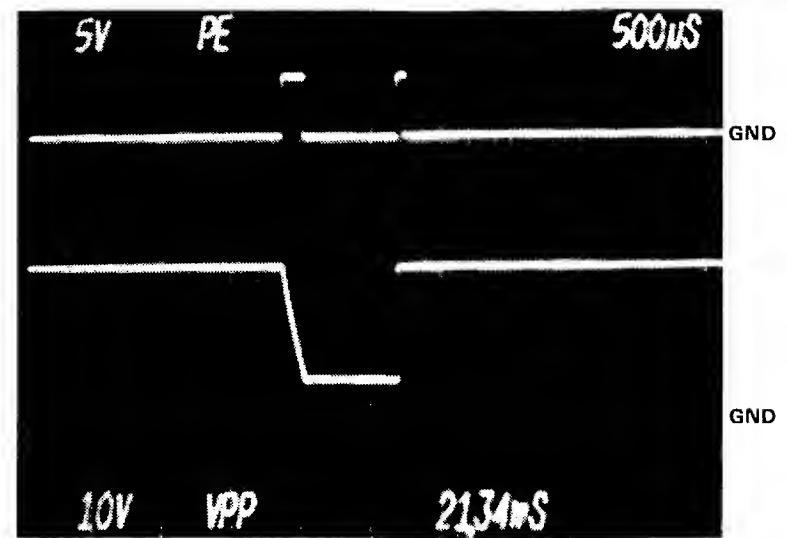
TIMING DIAGRAM

FAMILY CODE B3

Sheet 2 of 3 **DATA I/O**



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# REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	See Sheet 1		

TIMING DIAGRAM

FAMILY CODE B3

Sheet 3 of 3

**DATA I/O**

## SECTION 5

# CIRCUIT DESCRIPTION

### 5.1 INTRODUCTION

This section describes the 22A programmer's circuitry. It includes a general discussion of the programmer's architecture and a more specific description of the 22A's main circuitry functions. These functional groupings of circuitry are described in section 5.3. Each grouping (except socket adapter) is described in its own subsection along with a functional block diagram of the circuitry. Refer to the individual socket adapter manual for a complete circuit description of that adapter. In some cases, the circuitry function is located on more than one circuit board. This division is clearly indicated on the block diagram and in text.

### 5.2 ARCHITECTURE

The programmer is a microprocessor-based system using bus architecture. It is designed around a 68A09 microprocessor chip. The processor is located on the Controller Board (702-1775). Figure 5-1 is the system block diagram.

#### 5.2.1 THE BUS

The bus consists of a 16-bit address bus, 8-bit data bus, power supply lines and control lines. The bus assignments are detailed in table 5-1 and figure 5-3. All communications between portions of the circuitry are handled in the same manner over this bus. Timing of read and write operations is shown in figure 5-2.

Table 5-1. I/O Address Map

ADDRESS	FUNCTION
CC00-CC3F	Non volatile RAM
CC40-CC41	Keyboard/display
CC80-CC83	Serial port
CD00-CD17	Hybrid data control registers
CD18-CD1F	CE control registers
CD20-CD2F	Address registers 1 and 2
CD30-CD37	Control register 3
CD38	Program current DAC
CD39	Clamp supply DAC
CD50	Pulse generator
CD68	Signature Verifier (ST3)
CD70	Signature Verifier (ST2)
CD80-CD87	Control register 1
CD88	Non volatile store
CD90-CD97	Control register 2
CD98	Read gate 1
CDA0	Read gate 2
CDA8	VCC voltage DAC
CDA9	VCC current DAC
CDB0	Bit supply DAC
CDB1	CE supply DAC
CDB8	Comparator reference DAC
CDB9	Variable load DAC

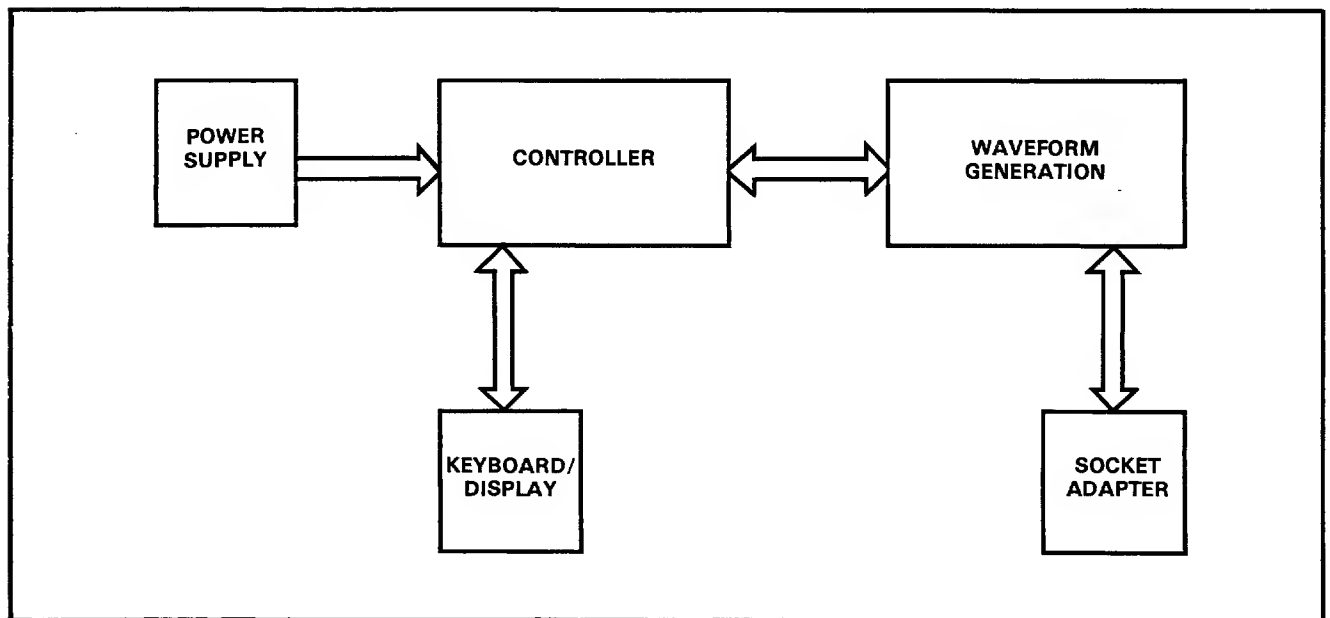
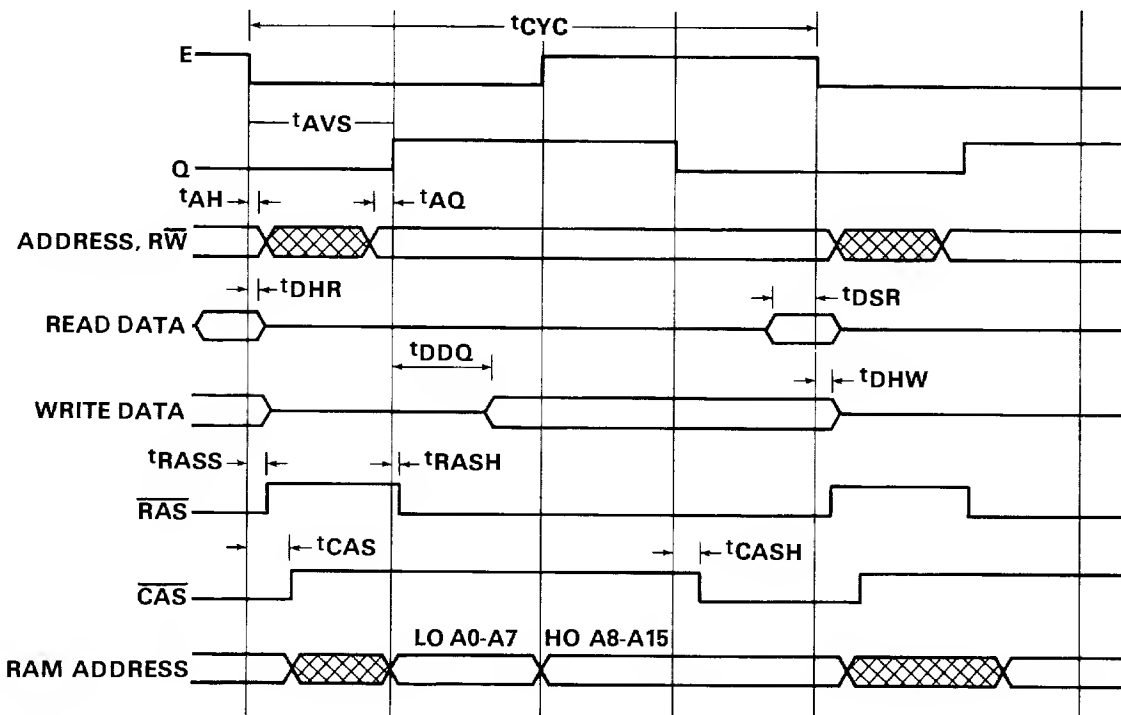


Figure 5-1. System Block Diagram



Parameter	Symbol	Minimum	Nominal	Maximum	Units
Cycle time	$t_{CYC}$		789		ns
Delay, E to Q rise	$t_{AVS}$	130		165	ns
Address hold time	$t_{AH}$	20			ns
Address valid to Q rise	$t_{AQ}$	25			ns
Read data hold time	$t_{DHR}$	10			ns
Read data setup time	$t_{DSR}$	60			ns
Data delay from Q	$t_{DDQ}$			149	ns
Write data hold time	$t_{DHW}$	30			ns
E to RAS delay time	$t_{RASS}$			59	ns
Q to RAS hold time	$t_{RASH}$			15	ns
E to CAS delay time	$t_{CASS}$			89	ns
Q to CAS hold time	$t_{CASH}$			30	ns

Figure 5-2. Bus

### 5.2.2 ADDRESS MAP

The address map (figure 5-3) shows the location, in hexadecimal, of each decoded function of the programmer. Table 5-1 is an expansion of the I/O portion.

### 5.2.3 HARDWARE INTERCONNECTION

Figure 5-4 illustrates the hardware interconnection of the primary assemblies on the 22A.

### 5.3 MAIN CIRCUITRY FUNCTIONS

The following is a functional description of the 22A's circuitry. The circuitry is divided into five main functions: power supply, keyboard/display, socket adapters, controller and waveform generation. In some cases, the circuitry function may overlap from one circuit board to another. When this occurs, this transition is clearly labeled on the block diagram for that circuitry function. Schematics for all circuit boards are located in Appendix D.

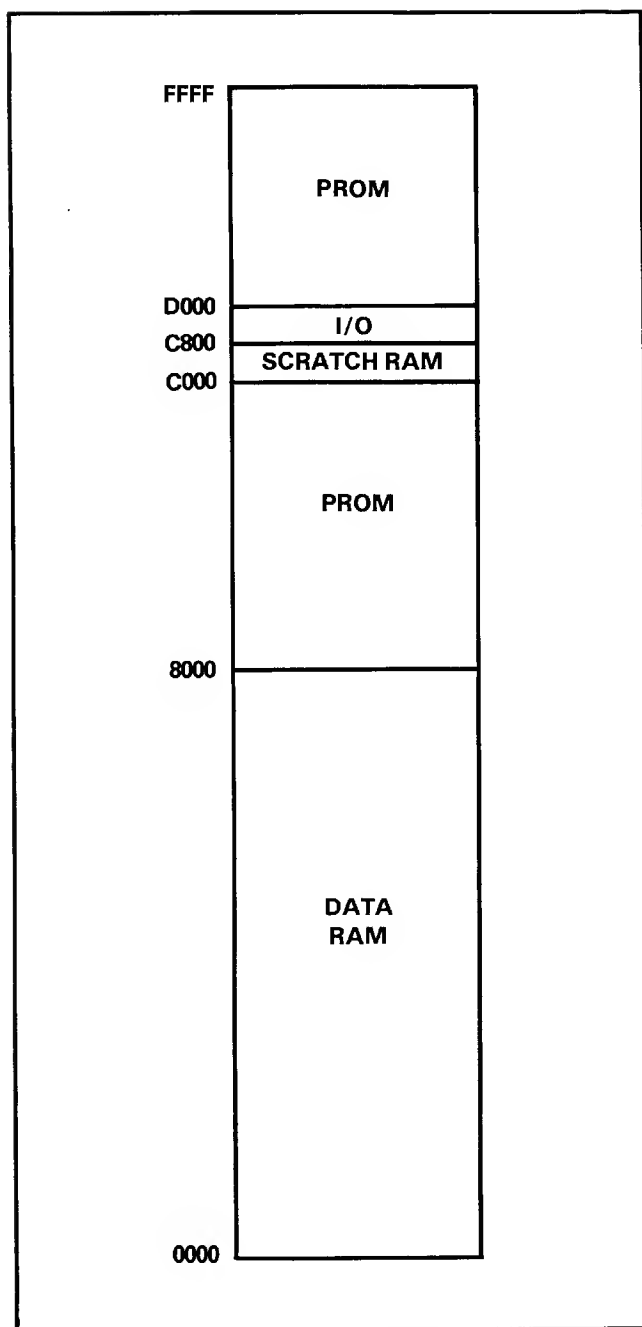


Figure 5-3. Address Map

### 5.3.1 POWER SUPPLY

The power supply is divided into two main sub-assemblies: the transformer cable assembly (709-0091) and the power supply assembly (702-1774). Refer to figure 5-5. These sub-assemblies are described in this subsection.

### Transformer Cable Assembly

The transformer cable assembly is made up of the AC line filter, AC line fuse, power switch, voltage selector and transformer. The AC line filter, line fuse and voltage selection wheel are all in a single unit. The voltage selector unit adapts the programmer to the correct line voltage. This AC line voltage selection process is described in section 2.4.1. The transformer primary contains taps which provide for operation at 100, 120, 220 or 240 volts.

### Power Supply Regulator

The transformer secondary is applied through fuse network F1 through F11 and is sent to the rectifier, filter and regulator network. Replacing fuses F1 through F4 is a simple procedure. Disassemble the programmer according to figure 4-1. Now that you have gained access to the inside of the programmer, the fuses snap easily in and out of their holders. Table 5-2 provides the amperage for each of these fuses.

The - 15 and + 48 volts are unregulated supplies rectified by diodes CR1 through CR4 and CR5 through CR8; and filtered by capacitors C4 and C5. The + 25 volts is a regulated supply rectified by diode CR9 through CR12, filtered by capacitor C1 and regulated by the three-terminal regulator VR2. The output of the + 25 volt supply is further regulated by VR1 to provide a + 15 volt supply. This + 15 volt supply is applied through fuse 11 to the center tap of the secondary winding. The other two legs of this winding provide 5.5 volts AC to the filaments of the FIP (fluorescent indicator panel) display. The + 5 volts is a regulated supply rectified by diodes CR13 through CR16 and filtered by capacitors C2 and C3 and regulated by VR3. Regulator VR3 is located on the back panel and is connected to the power supply by the regulator cable (709-0093).

### Fan

The fan connects to the transformer cable assembly and provides cooling to the internal circuitry of the 22A.

Table 5-2. Power Supply Fuse Requirements, F1-F4

Fuse Number	Fuse Type	Supply
F1	0.5A 250V slow blow	- 15V
F2	1A 250V fast blow	+ 48V
F3	2A 250V fast blow	+ 25V
F4	8A 125V fast blow	+ 5V

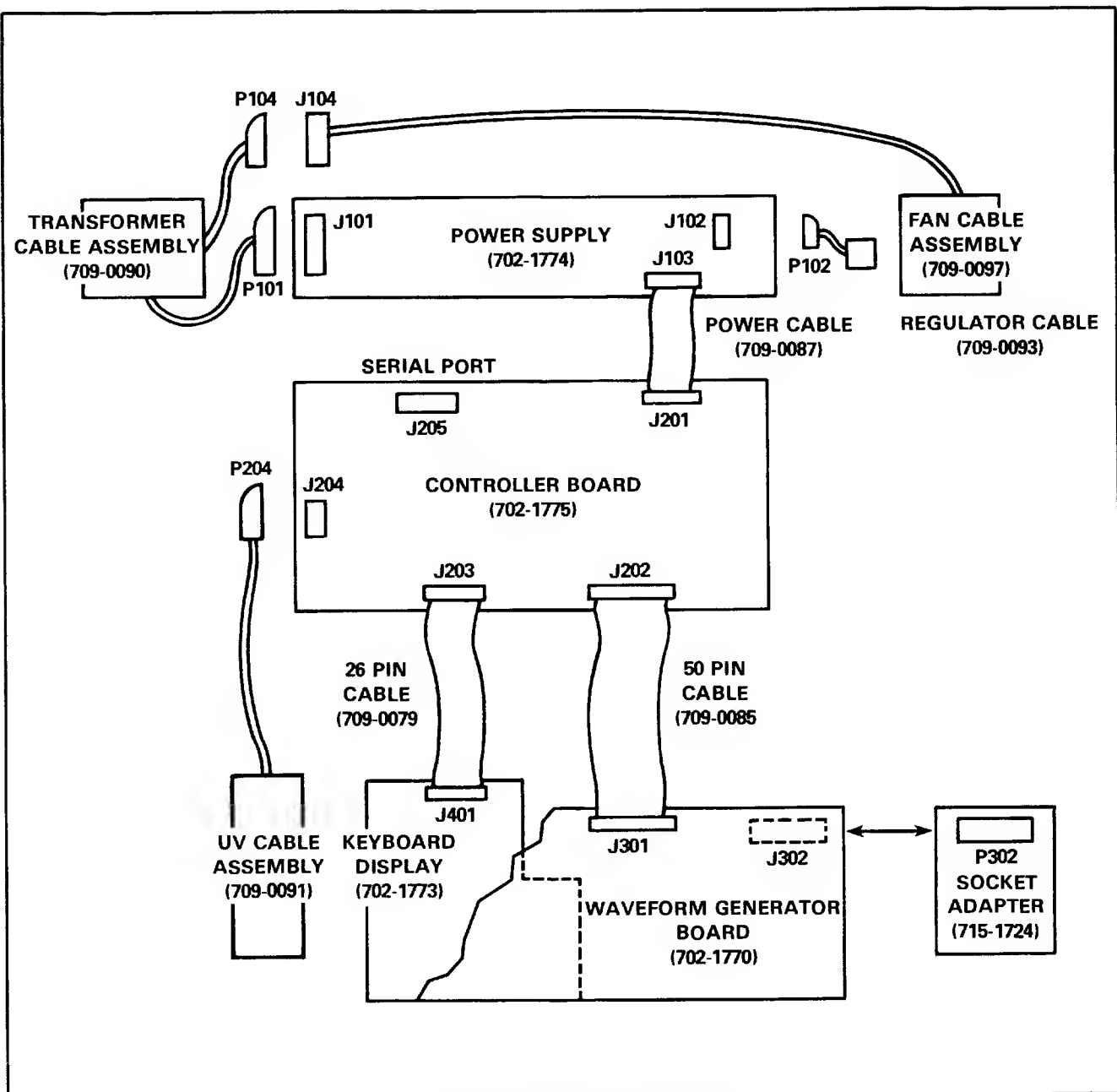


Figure 5-4. Interconnection Diagram



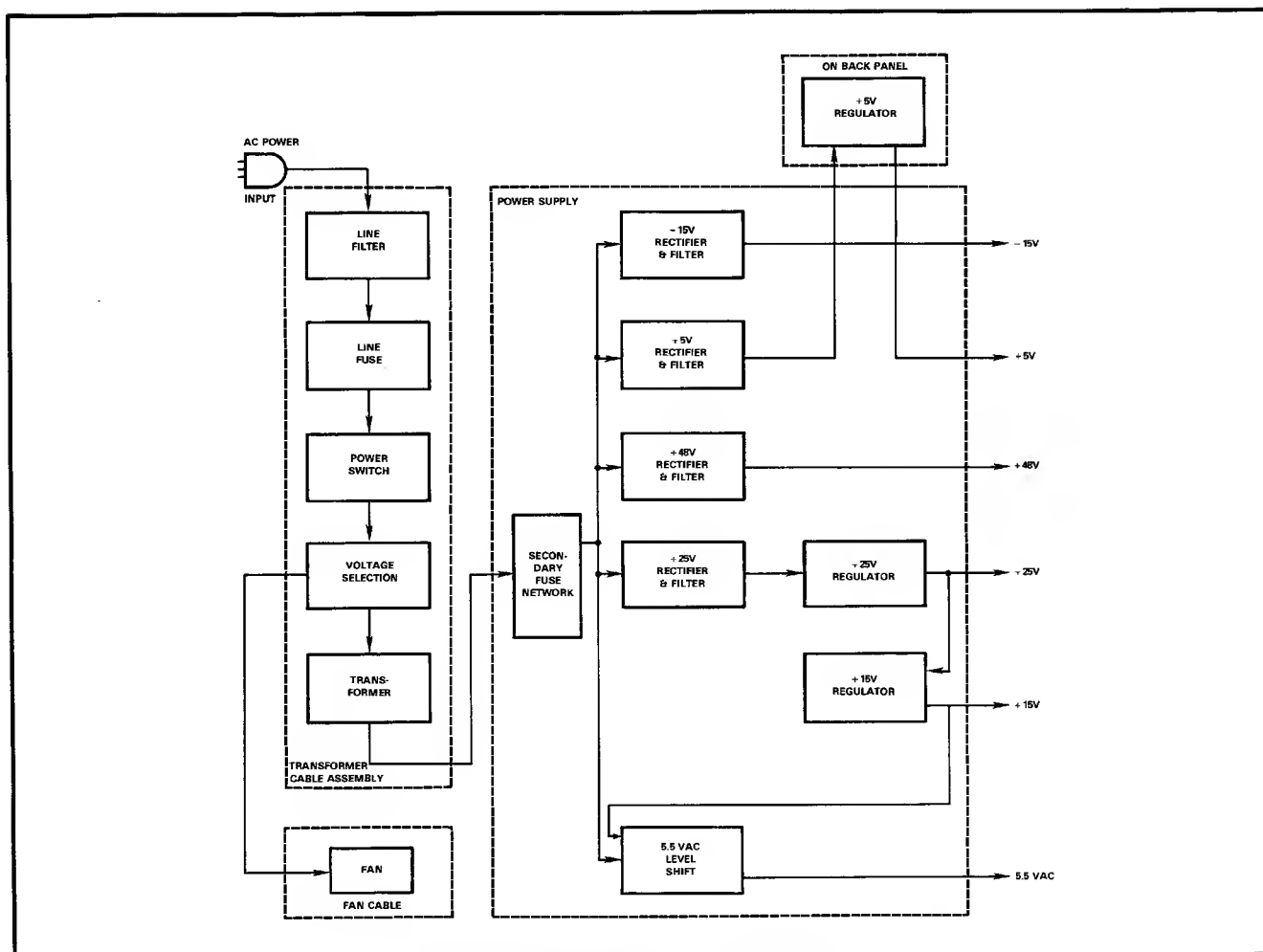


Figure 5-5. Block Diagram, Power Supply

### 5.3.2 KEYBOARD/DISPLAY

The keyboard/display circuitry function is illustrated in figure 5-6 and described in the following paragraphs.

#### Keyboard/Display Controller

The keyboard/display controller chip U49 is physically located on the Controller board and provides the necessary interface signals for the display and the keyboard.

#### Keyboard Drive

Scan lines on the controller U49, SL0 through SL3, are decoded by U15 and applied to the matrix of keys.

#### Keyboard

Commands from the matrix of keys are returned to the controller U49 by way of return lines RL0 through RL3 and RL7.

#### Display Drive

The signals for the FIP display originate from the controller outputs A0, A1, and B0 through B3. These signals are applied to the character generator PROM (U13). The character generator PROM outputs control the data segments that appear in the display. This data is timed by decoder U12 and counter U14 and is applied to display latches U3 through U6. Segment drive U10 and U11 level shift the outputs of the display latches to the voltages required by the FIP display inputs. The four scan lines from the controller (SL0 through SL3) are decoded by U1 and U2. These lines are level shifted by digit drive U8 and U9 to provide the necessary digit select signals.

#### FIP (Flourescent Indicator Panel) Display

The FIP is a 16 character alpha numeric display.

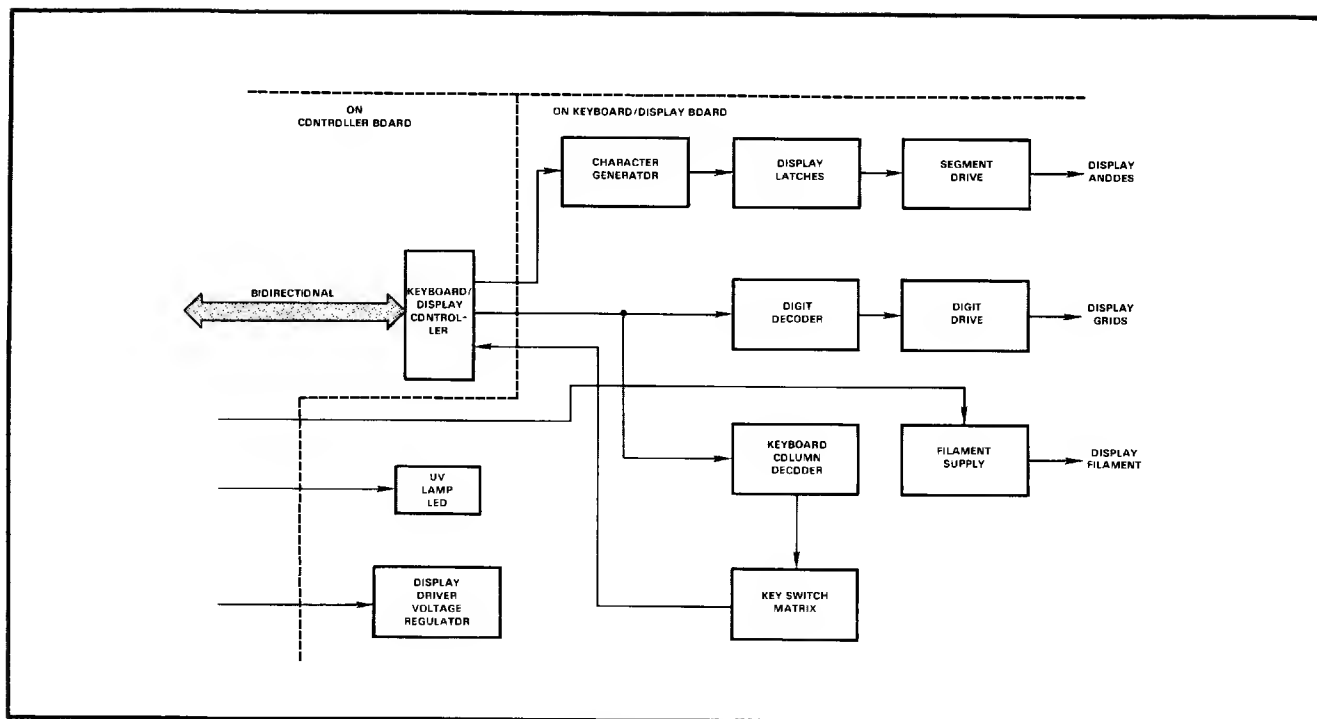


Figure 5-6. Block Diagram, Keyboard/Display Function

### 5.3.3 SOCKET ADAPTERS

The dual 20-pin socket adapter (351A-064) is a standard feature of the 22A. There are also three other optional socket adapters available on the 22A: 351A-074 (24-pin skinny wide devices), 351A-075 (Intel 8741, 8742, 8748, 8748H, 8749H, 8750H, 8755A) and 351A-076 (Intel 8751). These socket adapters contain clamp diode networks for noise suppression and some may contain circuitry to provide voltage level shifting. Consult the circuit description section of the individual socket adapter manual for complete details.

### 5.3.4 CONTROLLER

The following is a description of Controller board (702-1775). The circuitry functions of the 22A Controller board are described in this section and illustrated in figure 5-7.

#### Microprocessor Decode and Memory

The 22A uses a 68A09 microprocessor. The processor clock is generated with crystal Y1 and inverter U1. The power-on reset circuit CR3, Q10 and U8 provide a reset for the processor and an array recall signal for the non volatile RAM U37. The microprocessor's address bus is decoded by PROM U9 and decoders U13, U22 and U14. Program memory is provided with two on-line PROMs (U18 and U19) and three page PROMs (U15 through U17). Page selection of these PROMs is provided through U20 and control register U11. The microprocessor's scratch and non volatile RAM is provided by U36 and U37.

#### Data RAM

The 22A contains up to 64K x 8 bits of dynamic data RAM. Refresh for the dynamic RAM is generated by signals from the microprocessor using gates U43 and U44, address multiplexers (U34, U35, U41, U45) and refresh counter U40. The RAM is divided into two pages which overlay the same address space. Page selection is provided by control register U11.

#### Serial Port

U6 is the RS232 compatible serial interface device. The interface signals from U6 are shifted to the proper RS232 levels by interface U4 and U5 and are then routed to the serial port connector. Transistors Q5 and Q6 provide a switch for use with a Data I/O Serial Paper Tape Reader. This switch is turned on automatically during a copy or verify operation from port to RAM.

#### UV Lamp

The UV lamp power is derived from the 25-volt supply, routed through transistor switch Q3 and Q4 and then inverted by transformer T1 and transistor switches Q1 and Q2. The voltage present at the transformer secondary, a 20-kilohertz 35-volt peak AC wave, is limited by inductor L1 and applied to the terminals of the UV lamp. The lamp is physically located on the UV lamp assembly on the front panel. When the UV lamp is first turned on, a three second start signal is provided by relay K1. This start signal

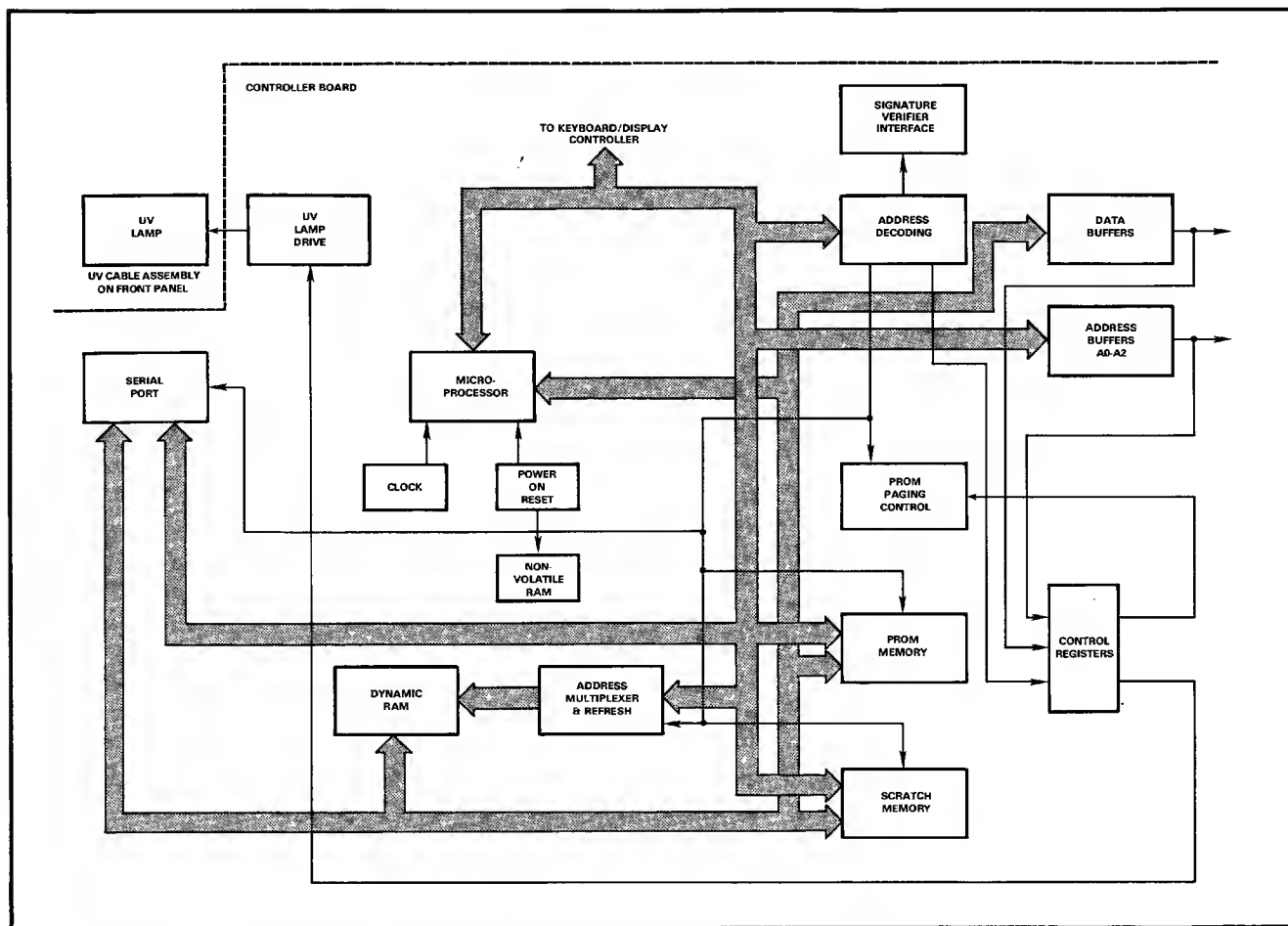


Figure 5-7. Block Diagram, Controller Board

connects the two filaments of the UV lamp in series causing them to heat and ionize the gas inside the tube. Zener diodes CR17 and CR18 provide noise suppression when relay K1 opens. Diode CR19, transistor Q17 and gate U43 provide a TTL signal to sense the state of the UV lamp.

#### Address and Data Buffers

The three lower address lines (A0 through A2) are buffered by register U10. The data lines are buffered by register U53. These two registers provide isolation between the processor and I/O devices.

#### Control Registers

The control registers (U11 and U21) provide the necessary control signals for other functions on the controller. The controller board also contains a signature verifier interface (U64) which provides start and stop signals for signature verification.

#### 5.3.5 WAVEFORM GENERATION

Waveform generation circuitry is located both on the Waveform Generator board and the Controller board. This division of circuitry is noted in figure 5-8.

#### Device Voltage Supplies

The device voltage supplies include: VCC, bit and chip enable (CE), VBB, pull-up/pull-down, V reference and -9 volts.

The VCC voltage is generated by DAC U61 op amp U31 and U30 and pass element Q13. The VCC current limit is adjustable by DAC U61, op amp 31 and potentiometer R70. The VCC voltage can be routed to any of three pins by the VCC switches consisting of Q14 through Q16. Depending upon which VCC switch is on, the proper feedback is selected through gates U62 and analog switch U63. This feedback path returns via potentiometer R65 to the input of op amp U30.

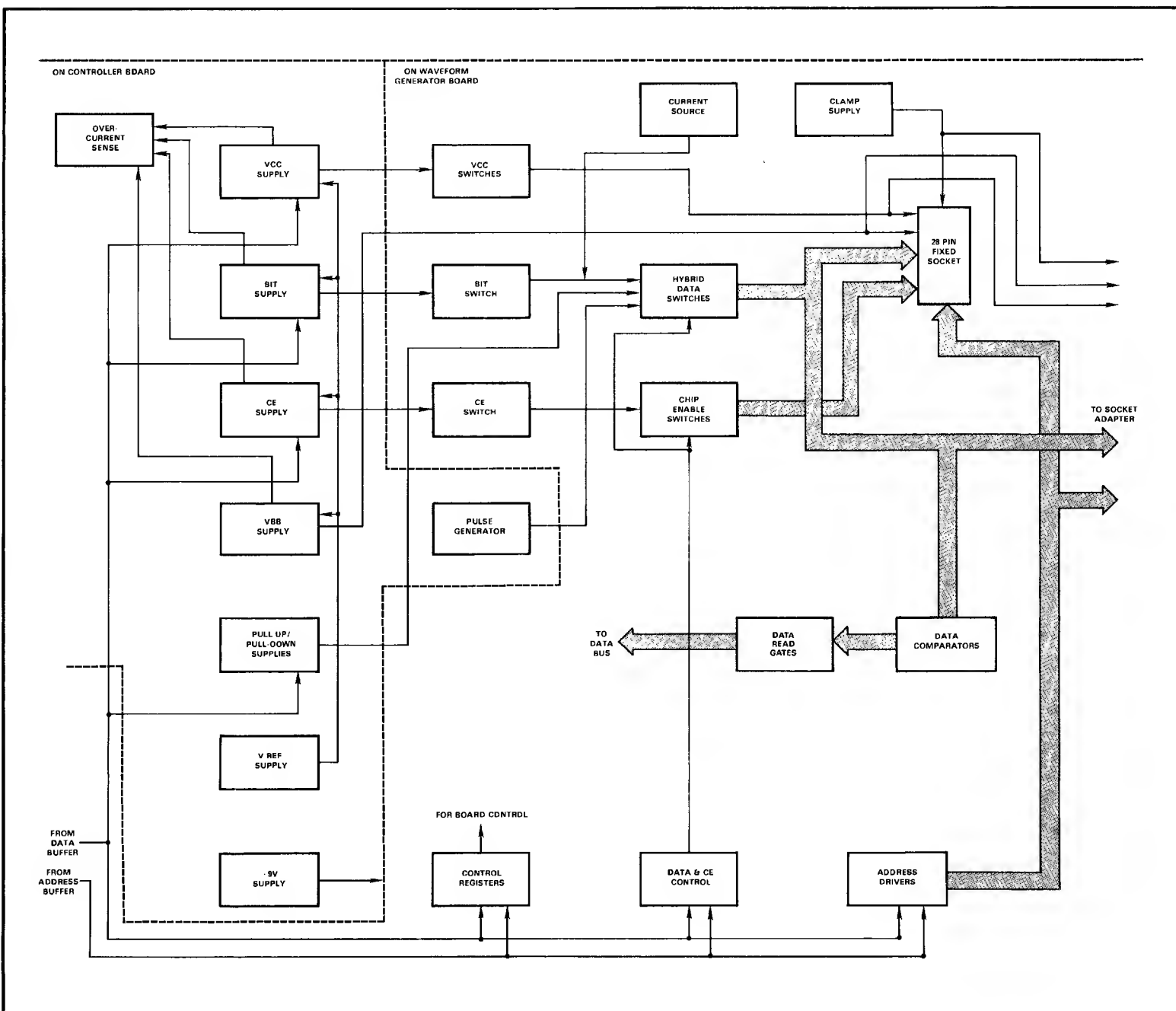


Figure 5-8. Block Diagram Waveform Generation

The voltage for the bit and CE supplies is generated from DAC U59 through op amps U28, U27 and U29 and pass elements Q7 and Q12, respectively.

The fixed voltage VBB supply is generated from the reference through op amp U25, pass element Q9 and switch Q10.

The variable voltage load for pull-up supply is generated from the B side of DAC U57 through op amps U26 and pass element Q11 and switched load supply switch Q8. The pull-down network originates on the waveform generator board from transistor Q14. These pull-up/pull-down supplies are applied to the hybrid network providing a variable load to the data lines.

The voltage reference (V Reference) provides a stable 5 volt reference for other waveform generation circuitry. It consists of regulator VR2 and transistor Q8.

The -9 volt supply is provided by regulator VR1 and provides a negative reference voltage for other waveform generation circuitry.

### Device Current Supplies

Both the programmable current source and the 20mA current source, together with the clamp supply, are located on the Waveform Generator board. The programmable current source is generated from the A side of DAC U18 through op amps U17 and transistor Q9. The level of current is set by resistors R11 and potentiometer R20. The programmable current source is turned on by gate U28 at pin 13. The 20mA current source is generated from regulator VR1 and transistor Q9. The 20mA current level is set with resistor R14 and potentiometer R21 and is turned on by transistor Q22. The current level for both the programmable and 20mA current sources are generated by op amp U27 and transistor Q11 from the voltage input present at U27 pin 3. The clamp supply is generated from the B side of DAC U18 through op amps U17, U31 and U19 and pass transistor Q10. The output of the clamp supply at TP4 is routed to the diode network on the 28-pin socket (or socket adapter) to provide noise suppression.

### Device Switching Generation

Device switching generation consists of: pulse generator, bit switch, CE switch, hybrid data switches and CE switches.

The pulse generator is located on the Controller board. The function of the pulse generator is to produce short duration pulses that are too fast to be generated by the microprocessor. The width of these pulses is determined by the data in register U55. The data is parallel loaded into counters U54 and U56. A pulse generator comprised of crystal Y2 and gates U50 is applied to the clock inputs of counters U54 and U56. The pulse begins when a read strobe occurs at gate U51, pin 12 or 13. This will load counters U54 and U56 and allows them to count until a carry is generated which terminates the pulse. This pulse signal is also applied to the read gates on the Waveform Generator board which

latches in the data from the device through the comparator network. This allows data to be read from the device at a precise time after the previous pulse is generated.

The bit and CE switches turn the bit and CE voltage level supplies on and off. They provide a variable controlled rise rate to both the bit and CE switch outputs.

Each of the six hybrid circuits drives two pins, which may either be address or data lines, depending upon the pinout of the device. Half of the hybrid functions as a pin driver to steer the output of the bit switch to the proper pin on the socket or socket adapter. It can also generate a TTL level signal on these pins. These six hybrids (U10 through U15) are in 20-pin single in-line packages. Hybrid data switches get their input signals from registers U3 through U5.

The four chip enable switches drive the chip enable lines on the socket (or socket adapter). These switches get their TTL input signals from register U2. A typical chip enable switch functions to pass the output of the CE switch through transistor Q33 which is turned on by transistor Q31 and Q32; transistors Q30 and Q26 function as a TTL level driver.

Other miscellaneous circuitry contained on the Waveform Generator board consists of a 12-volt write enable signal generated by gates U28-U29 and zener diode CR65. The hybrids receive a -9/-3 volt base drive signal from transistors Q12-Q13 and zener diode CR36.

### Device Read Circuitry

The device read circuitry consists of the data comparators and an overcurrent sense network.

Data coming from the fixed 28-pin front panel socket (U16) or socket adapter is routed to the data comparator U20 through U23. The sense level of these comparators is set by the comparator supply located on the Controller board. This comparator supply is generated from the A side of DAC U57 and ends up at U26. The outputs of the comparators are accessed by the data read gates U25 and U26.

The overcurrent sense network will cause a shut-down of the supply voltages if an overcurrent condition is detected in any of four supplies: VCC, bit, CE or VBB. This sense network is located on the controller and consists of comparator U60, gate U24, integrator R121 and C58. The output of the integrator is routed to the clear line of U21, a controller register. When an overcurrent condition occurs, it will clear this register (U21) causing all its outputs, including the output tied to gate U51 pin 10, to go low. The output of this gate, called the overcurrent clear line, is routed to the Waveform Generator board and causes a clear condition to all the control registers. This shuts down all the voltages on the Waveform Generator board. The microprocessor will sense that an overcurrent shut down has occurred. It does this by reading the level of the V reference supply through comparator U20 pin 11. If an overcurrent shut down has occurred, the V Reference voltage will be 0.

# APPENDIX A

## DATA TRANSLATION FORMATS

### A.1 INTRODUCTION

This appendix defines the data translation formats available for the 22A. The 22A is capable of interfacing with all RS232C serial equipment employing a data translation format described in this appendix.

Each data translation format is assigned a 2-digit code which the operator enters into the programmer (from the keyboard or, in remote control, through the serial port) to send or receive data in that format. In addition to the data translation format code, there is a 1-digit instrument control code which specifies control characters to be transmitted to, or received from, peripheral instruments.

### A.2 DATA VERIFICATION

For data verification the 22A calculates a sum-check of all data sent to or from the programmer. At the end of a successful input operation, the programmer will display the sum-check of all data transferred. It will also compare any received sum-check fields with its own calculation. If the two agree, the programmer will display the sum-check; a mismatch will produce an error message. Output data is always followed by a sum-check field which may be printed on disk or tape for use in subsequent input operations.

### A.3 CODES

Each format is assigned a 2-digit data translation format code which the operator enters into the programmer to transfer data in that format. In addition to this code, a 1-digit instrument control code may be used to specify control characters for peripheral equipment. The codes must be formatted as shown in figure A-1. If no codes are entered into the programmer, the current default values will be in effect.

See table A-1 for a definition of instrument control codes and table A-2 for a definition of data translation format codes.

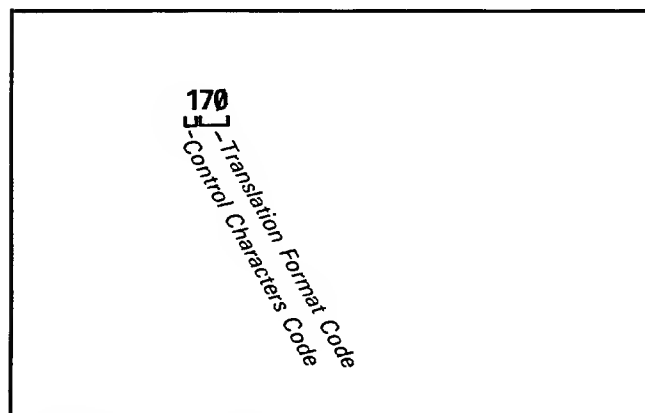


Figure A-1. Formatting the Instrument Control Code and Data Translation Format Code

Table A-1. Instrument Control Codes

CONTROL CODE	PROGRAMMER ACTION
0	No control character sent.
1	Send "reader on" (ASCII DC1/Hex 11) when ready to receive data, and "reader off" (ASCII DC3/Hex 13) when all data is received. Also send "punch on" (ASCII DC2/Hex 12) before sending data, and "punch off" (ASCII DC4/Hex 14) after sending data.
2	Sends data after acknowledging a "reader on" (ASCII DC1/Hex 11), and stops sending data after acknowledging a "reader off" (ASCII DC3/Hex 13).

### A.4 TRANSLATION FORMATS

This section gives information on the translation formats available for input and output by the 22A.

#### A.4.1 BINARY TRANSFER, CODE 10

Data transfer in the Binary format consists of a stream of 8-bit data words preceded by a byte count and followed by a sum-check. The Binary format does not have addresses.

A paper tape generated by a programmer will contain a 5-byte, arrow-shaped header followed by a null and a 4-nibble byte count. The start code, a nonprintable rubout in even parity, follows the byte count. The end of data is signalled by 2 nulls and a 2-byte sum-check of the data field. Refer to figure A-2.

The programmer stores incoming binary data upon receipt of the start character. Data is stored in RAM starting at the first RAM address and ending at the last incoming data byte. Transmission may be aborted by pressing any mode key.

#### A.4.2 DEC BINARY FORMAT, CODE 11

Data transmission in the DEC Binary format is a stream of 8-bit data words with no control characters except the start code. The start code is one null preceded by at least one rubout. A tape output from the programmer will contain 32 rubouts in the leader. The DEC Binary format does not have addresses.

#### A.4.3 ASCII BINARY FORMAT, CODES 01, 02 and 03 (or 05, 06, and 07)

In these formats, bytes are recorded in ASCII codes with binary digits represented by N's and P's, L's and H's, and 1's and 0's, respectively. See figure A-3. The ASCII Binary formats do not have addresses.

Table A-2. Data Translation Formats

FORMAT	CODE
Binary	10
DEC Binary	11
ASCII-BNPF	01 (05)*
ASCII-BHLF	02 (06)*
ASCII-B10F	03 (07)*
5-Level BNPF	08 (09)*
Spectrum	12 (13)*
ASCII-Octal (Space)	30 (35) +
ASCII-Octal (Percent)	31 (36) +
ASCII-Octal (Apostrophe)	32
ASCII-Octal SMS	37
ASCII-Hex (Space)	50 (55) +
ASCII-Hex (Percent)	51 (56) +
ASCII-Hex (Apostrophe)	52
ASCII-Hex SMS	57
ASCII-Hex (Comma)	53 (58) +
RCA Cosmac	70
Fairchild Fairbug	80
MOS Technology	81
Motorola Exorciser	82
Intel Intellec 8/MDS	83
Signetics Absolute Object	85
Tektronix Hexadecimal	86
Motorola Exoramax	87
Intel MCS-86 Hexadecimal Object	88
Hewlett-Packard 64000 Absolute	89
Texas Instruments SDSMAC	90

\* For transmission of data without start codes, these alternate data translation format codes are used.

+ For transmission of data with the SOH (CTRL A) start code, these alternate data translation format codes are used.

Figure A-3 shows four data byte coded in each of the three ASCII Binary formats. Incoming bytes are stored in RAM sequentially starting at the first RAM address. Bytes are sandwiched between "B" and "F" characters and are normally separated by spaces. Any other characters, such as carriage returns or line feeds, may be inserted between an "F" and the next "B". The start codes are a nonprintable STX, control B (or hex 02 in "no parity"), and the end code is a nonprintable ETX, control C (or a hex 03 in "no parity").

**NOTE**

Data without a start code may be input to or output from the programmer by use of alternate data translation format codes. These are: ASCII-BNPF, 05; ASCII-BHLF, 06; ASCII-B10F, 07.

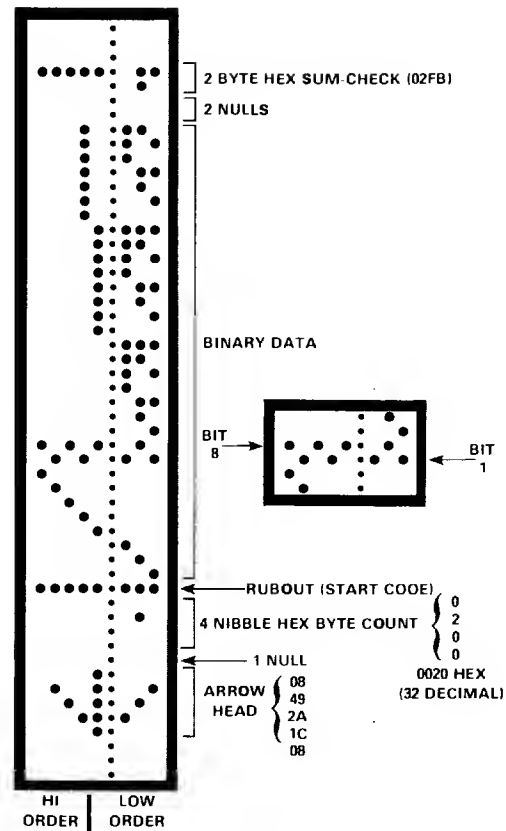


Figure A-2. Input or Output Binary Tape

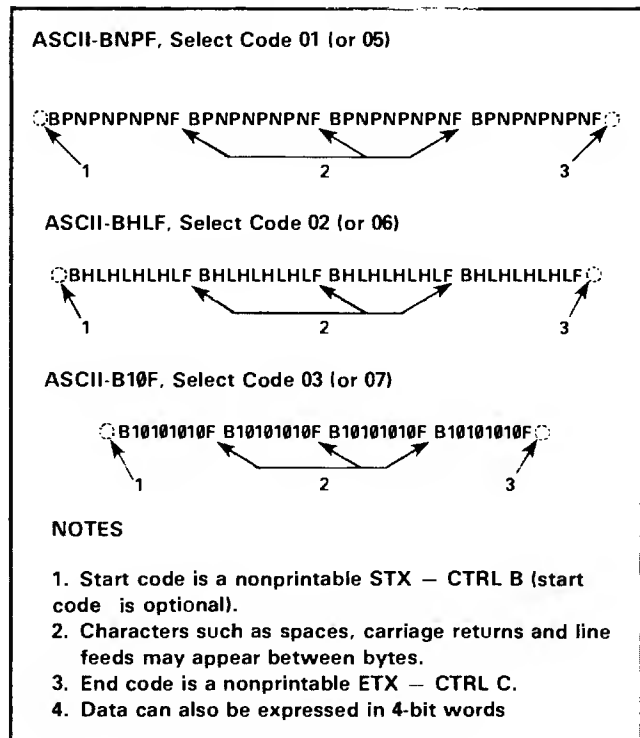


Figure A-3. ASCII Binary Formats

A single data byte can be aborted if the programmer receives an E character between B and F characters. Data will continue to be stored in sequential RAM addresses. The entire data transfer can be aborted by pressing any mode key (COPY, VERIFY, SELECT, EDIT).

Data is output in 4-byte lines with a space between bytes. The transmission is preceded and followed by 50 null characters.

#### A.4.4 5-Level BNPF FORMAT, CODES 08 or 09

Except for the start and end codes, the same character set and specifications are used for the ASCII-BNPF and 5-level BNPF Formats.

Data for input to the programmer is punched on 5-hole Telex paper tapes to be read by an ASCII-based reader that has an adjustable tape guide. The reader reads the tape as it would an 8-level tape, recording the 5 holes that are on the tape as 5 bits of data. The 3 most significant bits are recorded as if they were holes on an 8-level tape. The programmer's software converts the resulting 8-bit codes into valid data for entry in RAM.

The start code for the format is a left parenthesis, ("Figs K" on a Telex machine), and the end code is a right parenthesis, ("Figs L" on a Telex machine). The 5-level BNPF Format does not have addresses.

#### NOTE

*Data without a start code may be input to or output from the programmer by use of the alternate data translation format code, 09.*

#### A.4.5 SPECTRUM FORMAT, CODES 12 or 13

In this format, bytes are recorded in ASCII codes with binary digits represented by 1's and 0's. Each byte is preceded by an address.

Figure A-4 shows 2 data bytes coded in the Spectrum format. Bytes are sandwiched between the space and carriage-return characters and are normally separated by line feeds. The start code is a nonprintable STX, control B (or hex 02 in "no parity"), and the end code is a nonprintable ETX, control C (or hex 03 in "no parity").

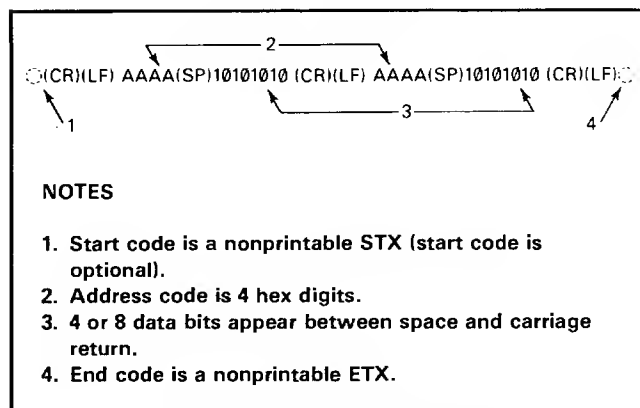


Figure A-4. Spectrum Format

#### NOTE

*Data without a start code may be input to or output from the programmer by use of the alternate data translation format code, 13.*

A single data byte can be aborted if the programmer receives an "E" character between a space and a carriage return. Data will continue to be stored in sequential RAM addresses. The entire data transfer can be aborted by pressing any mode key (COPY, VERIFY, SELECT or EDIT).

Data output to a printer will have one address and one byte of data on each line. The programmer first sends an STX (optionally), then the data, and finally an ETX. The transmission is preceded and followed by 50 null characters.

#### A.4.6 ASCII OCTAL & HEX FORMATS, CODES 30-37 and 50-58

Each of these formats has a start and end code, and similar address and sum-check specifications. Figure A-5 illustrates 4 data bytes coded in each of the 9 ASCII-Octal and Hex Formats. Data in these formats is organized in sequential bytes separated by the execute character (space, percent, apostrophe, or comma). Characters immediately preceding the execute character are interpreted as data. ASCII-Hex and Octal Formats can express 8-bit data, by 2 or 3 octal, or 1 or 2 hex characters. Line feeds, carriage returns and other characters may be included in the data stream as long as a data byte directly precedes each execute character.

Although each data byte has an address, most are implied. Data bytes are addressed sequentially unless an explicit address is included in the data stream. This address is preceded by a "\$" and an "A", must contain 2 to 4 hex or 3 to 6 octal characters, and must be followed by a comma, except for the ASCII-Hex (Comma) Format, which uses a period. The programmer skips to the new address to store the next data byte; succeeding bytes are again stored sequentially. See figure A-6.

Each format has an end code, which terminates input operations. However, if a new start code follows within 16 characters of an end code, input will continue uninterrupted.

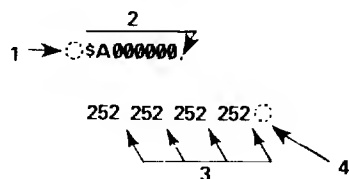
#### NOTE

*At least sixteen characters must follow an end code to avoid a timeout error.*

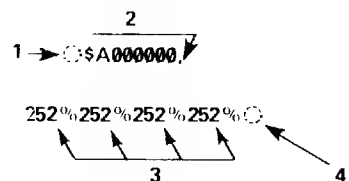
After receiving the final end code following an input operation, the programmer calculates a sum-check of all incoming data. Optionally, a sum-check can also be entered in the input data stream. The programmer compares this sum-check with its own calculated sum-check. If they match, the programmer will display the sum-check; if not, a sum-check error will be displayed. Specifications for the optional sum-check are given in figure A-7.



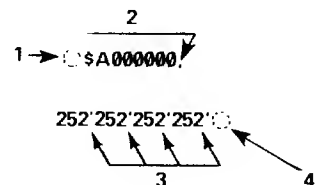
ASCII-Octal (Space), Select Code 30 (or 35)



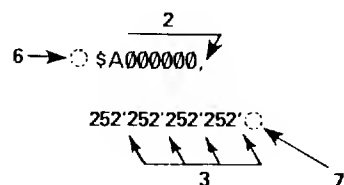
ASCII-Octal (Percent), Select Code 31 (or 36)



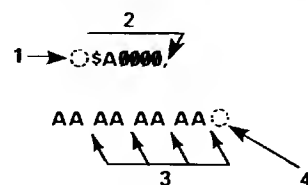
ASCII-Octal (Apostrophe), Select Code 32



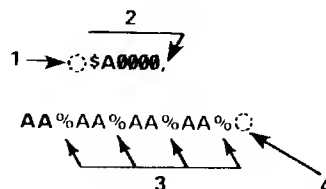
ASCII-Octal SMS, Select Code 37



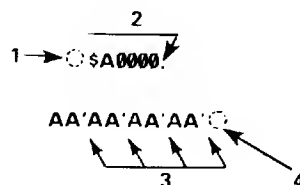
ASCII-Hex (Space), Select Code 50 (or 55)



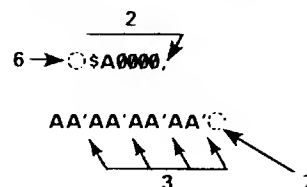
ASCII-Hex (Percent), Select Code 51 (or 56)



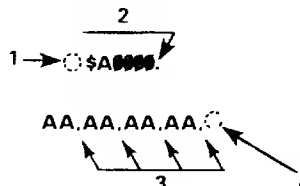
ASCII-Hex (Apostrophe), Select Code 52



ASCII-Hex SMS, Select Code 57



ASCII-Hex (Comma), Select Code 53 (or 58)



NOTES:

1. Start code is nonprintable STX — CTRL B (optionally SOH — CTRL A).
2. Optional address code may precede any data byte. Up to six address digits in octal formats, four in hex.

3. Execute code.
4. End code is a nonprintable ETX — CTRL C.
5. Data can also be expressed in 4-bit form.
6. Start code is nonprintable SOM — CTRL R.
7. End code is a nonprintable EOM — CTRL T.

Figure A-5. ASCII-Octal and Hex Formats

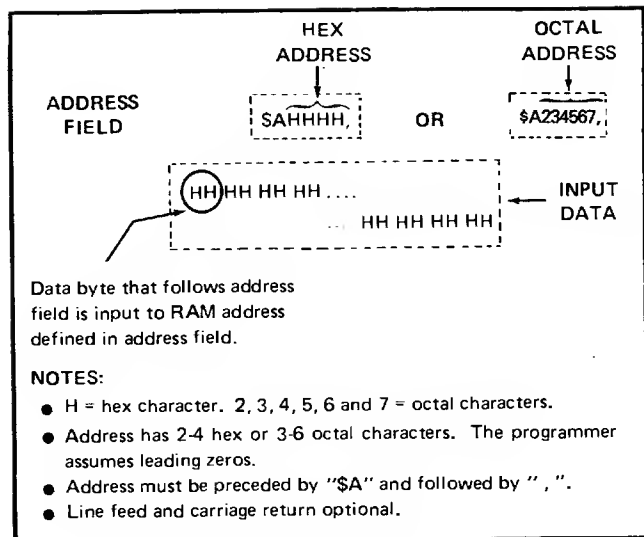


Figure A-6. Optional Address Field in ASCII-Octal and Hex Formats

Output is begun by invoking an output to Port operation. The programmer divides the output data into 8-line blocks.

Data transmission is begun with the start code, a nonprintable STX, optionally SOH.\* Data blocks follow, each one prefaced by an address for the first data byte in the block. The end of transmission is signalled by the end code, a nonprintable ETX. Directly following the end code is a sum-check of the transferred data. The transmission is preceded and followed by 50 null characters.

#### A.4.7 RCA COSMAC FORMAT, CODE 70

Data in this format begins with a start record consisting of the start character (!M or ?M), an address field, and a space. See figure A-8.

The start character ?M is sent to the programmer only by a development system. This happens when the operator enters the interrogation ?M at a terminal (linked in parallel with the programmer to the development system), followed by the address in the development system memory where data transmission is to begin, followed by a number of bytes to be transferred, then by a carriage return. The development system responds by sending ?M to the programmer, followed by the starting address, and a data stream which conforms to the data input format described in figure A-5. Transmission stops when the specified number of bytes have been transmitted.

Address specification is required for only the first data byte in the transfer. An address must have 1 to 4 hex characters and be followed by a space. The programmer records the next hex character after the space as the start

\* ASCII-Octal SMS and ASCII-Hex SMS use SOM (CTRL R) as a start code and EOM (CTRL T) as an end code.

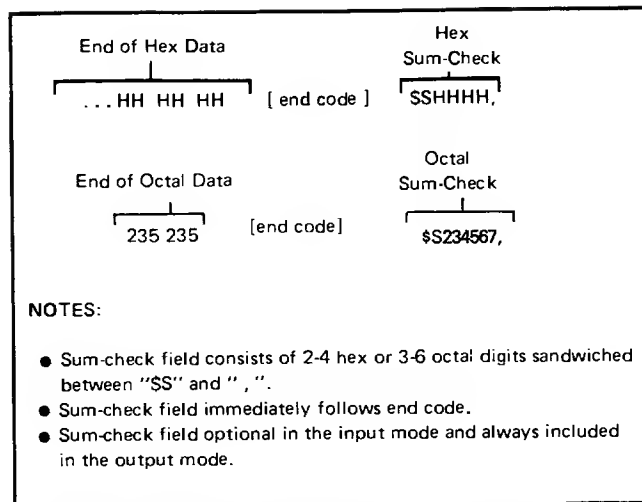


Figure A-7. Syntax of the Sum-Check Field in I/O Operations

of the first data byte. (A carriage return must follow the space if the start code ?M is used.) Succeeding bytes are recorded sequentially.

Each data record is followed by a comma if the next record is not preceded by an address, or by a semicolon if it starts with an address. Records consist of data bytes expressed as two hexadecimal characters and followed by either a comma or semicolon, and a carriage return. Any characters received between a comma or semicolon and a carriage return will be ignored by the programmer.

The carriage-return character is significant to this format because it can signal either the continuation or the end of data flow; if the carriage return is preceded by a comma or semicolon, more data must follow; the absence of a comma or semicolon before the carriage return indicates the end of transmission.

Output data records are followed by either a comma or a semicolon and a carriage return. The Start-of-File records are expressed exactly as for input. The transmission is preceded and followed by 50 null characters.

#### A.4.8 MICROPROCESSOR FORMATS

Data in these formats is organized into records characterized by expressed addresses and error-check codes. Each format has record start characters and sum-checks. Records are independent; that is, the programmer can accept addresses in nonsequential order. (The Fairchild Fairbug format differs from the other microprocessor formats in address setting. See the Fairchild Fairbug format description).

In the Fairbug format, input and output requirements are identical; both have 8-byte records and identical control characters. Figure A-9 simulates a Fairbug data file. A file begins with a 5-character prefix and ends with a 1-character suffix. The Start-of-File character is an "S", followed by the address of the first data byte. Each data byte is represented by 2 hexadecimal characters.

*Address specification is optional in this format; a record with no address directly follows the previous record.*

The programmer ignores any character (except for address characters) between a checksum and the start character of the next data record. These spaces can be used for any comments.

The last record consists of an asterisk only, which indicates the end of data transmission.



# • MOS TECHNOLOGY FORMAT, CODE 81

The data in each record is sandwiched between a 7-character prefix and a 4-character suffix. The number of data bytes in each record must be indicated by the byte count in the prefix. The input file can be divided into records of various length.

Figure A-10 simulates a series of valid data records. Each data record begins with a semicolon. The programmer

will ignore all characters received prior to the first semicolon. All other characters in a valid record must be valid hex digits (0-9, A-F). A 2-digit byte count follows the start character. The byte count, expressed in hexadecimal digits, must equal the number of data bytes in the record. The next 4 digits make up the address of the first data byte in the record. Data bytes follow, each represented by 2 hexadecimal digits.

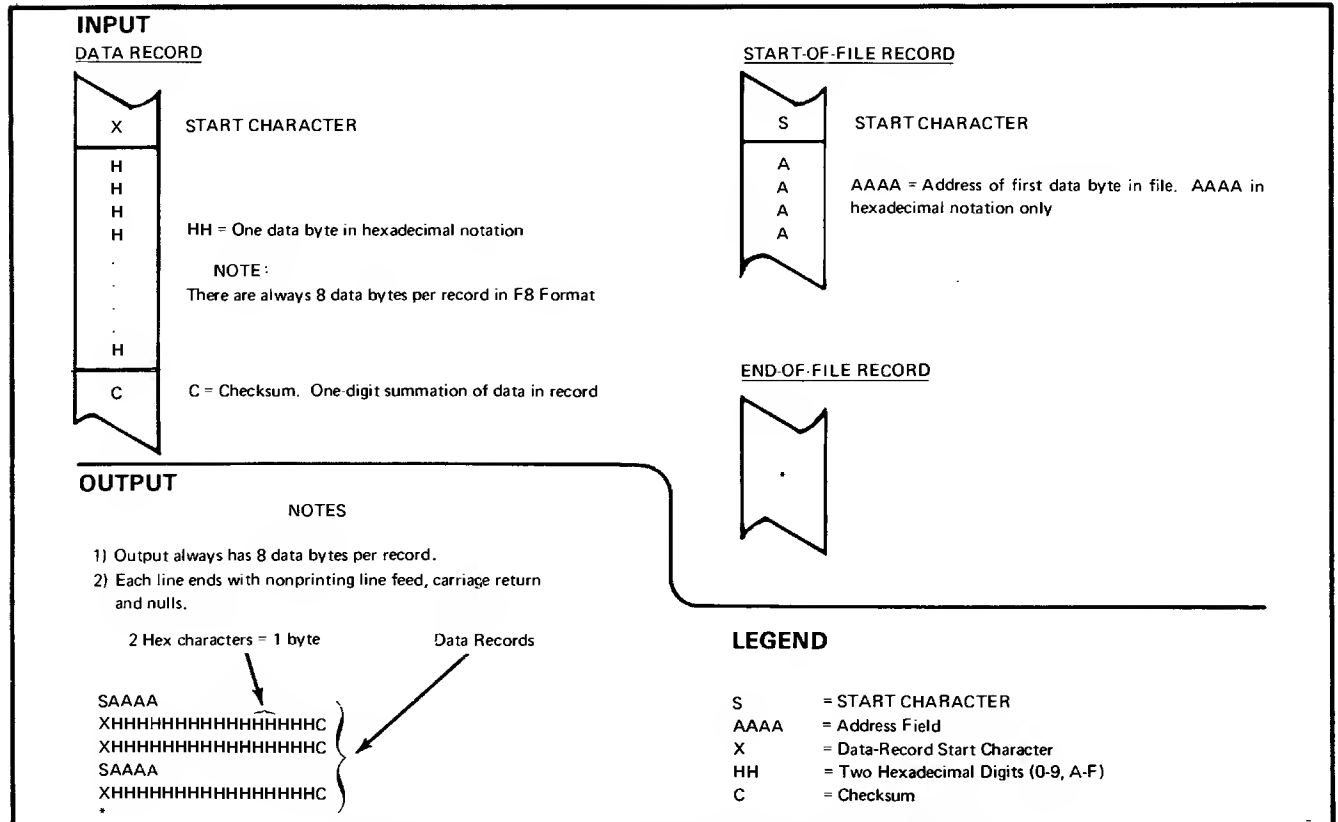


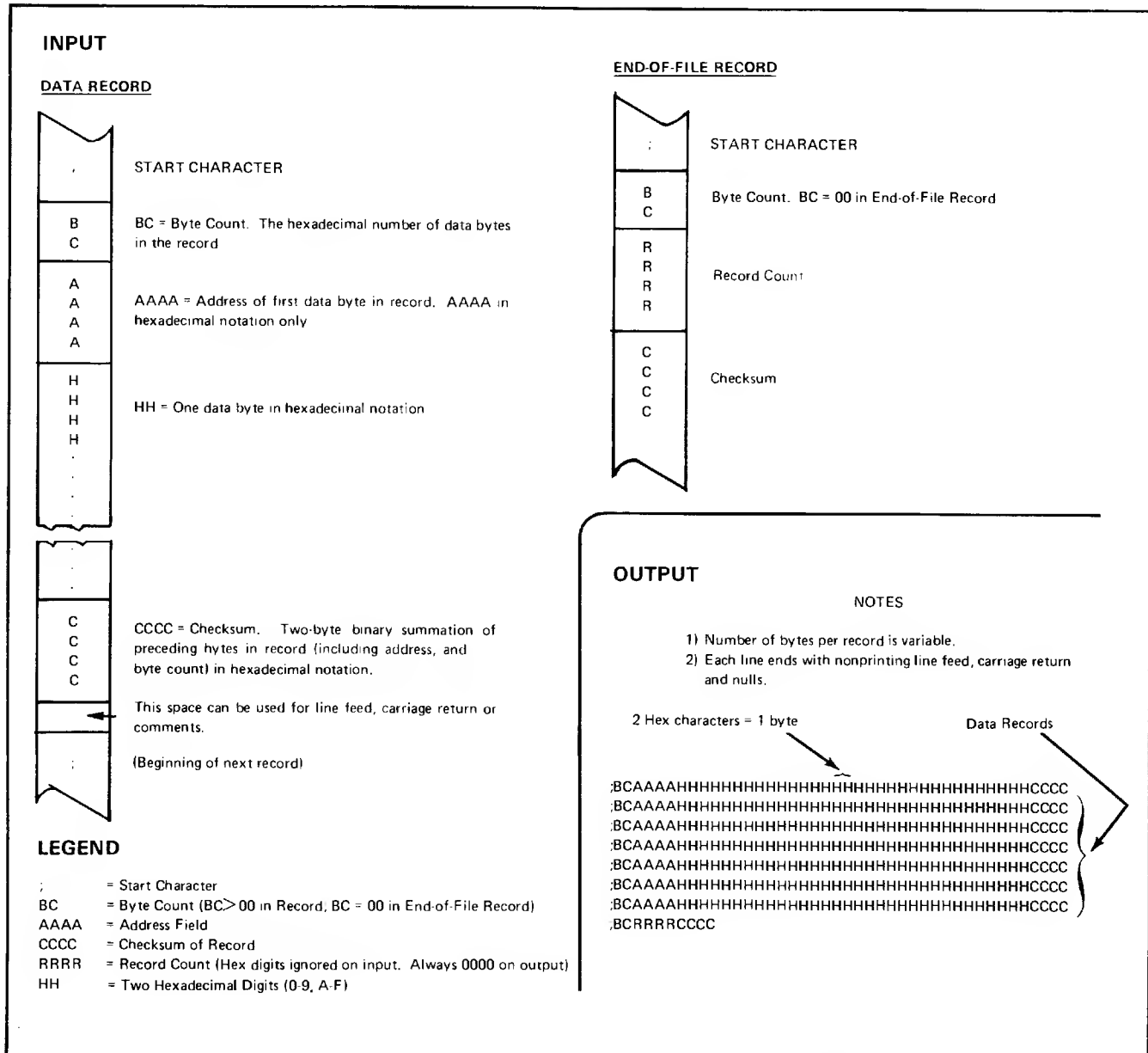
Figure A-9. Specifications for Fairchild Fairbug Data Files

- **MOTOROLA EXORCISER FORMAT, CODE 82**

Motorola data files may begin with a sign-on record, which is initiated by the code S0. Valid data records start with an 8-character prefix and end with a 2-character suffix. Figure A-11 demonstrates a series of valid Motorola data records.

Each data record begins with the start characters "S1"; the programmer will ignore all earlier characters. The third

and fourth characters represent the byte count, which expresses the number of data, address and sum-check bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix. Data bytes follow, each represented by 2 hexadecimal characters. The number of data bytes occurring must be 3 less than the byte count. The suffix is a 2-character checksum.



### Figure A-10. Specifications for MOS Technology Data Files

Intel data records begin with a 9-character prefix and end with a 2-character suffix. The byte count must equal the number of data bytes in the record.

**2-character byte count.** The 4 digits following the byte count give the address of the first data byte.

Each data byte is represented by 2 hex digits; the number of data bytes in each record must equal the byte count.



Figure A-13 shows the specifications of Signetics format files. The data in each record is sandwiched between a 9-character prefix and a 2-character suffix.

address check. Data is represented by pairs of hexadecimal characters. The byte count must equal the number of data bytes in the record. The suffix is a 2-character data check, calculated using the same operations described in figure A-13 for the address check.

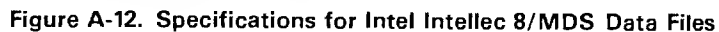


Figure A-14 illustrates a valid Tektronix data file. The data in each record is sandwiched between the start character (a slash) and a 2-character sum-check. Following the start character, the next 4 characters of the prefix express the address of the first data byte. The address is followed by a byte count, which represents the number of data bytes in the record, and by a sum-check of the address and byte count. Data bytes follow, represented by pairs of hexadecimal characters and succeeded by a sum-check of

Data is output from the programmer starting at the first RAM address and continuing until the number of bytes in the specified block has been transmitted. The programmer divides output data into records prefaced by a start character and an address field for the first byte in the record. The transmission is preceded and followed by 50 null characters.





## • MOTOROLA EXORMAX FORMAT, CODE 87

Motorola data files may begin with a sign-on record, initiated by the code S0. Data records start with an 8- or 10-character prefix and end with a 2-character suffix. Figure A-15 demonstrates a series of Motorola Exormax data records.

Each data record begins with the start characters S1 or S2—S1 if the following address field has 4 characters, S2 if it has 6 characters. The third and fourth characters

represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix (6 characters for addresses above hex FFFF). Data bytes follow, each represented by two hexadecimal characters. The number of data bytes occurring must be 3 less than the byte count. The suffix is a 2-character checksum.

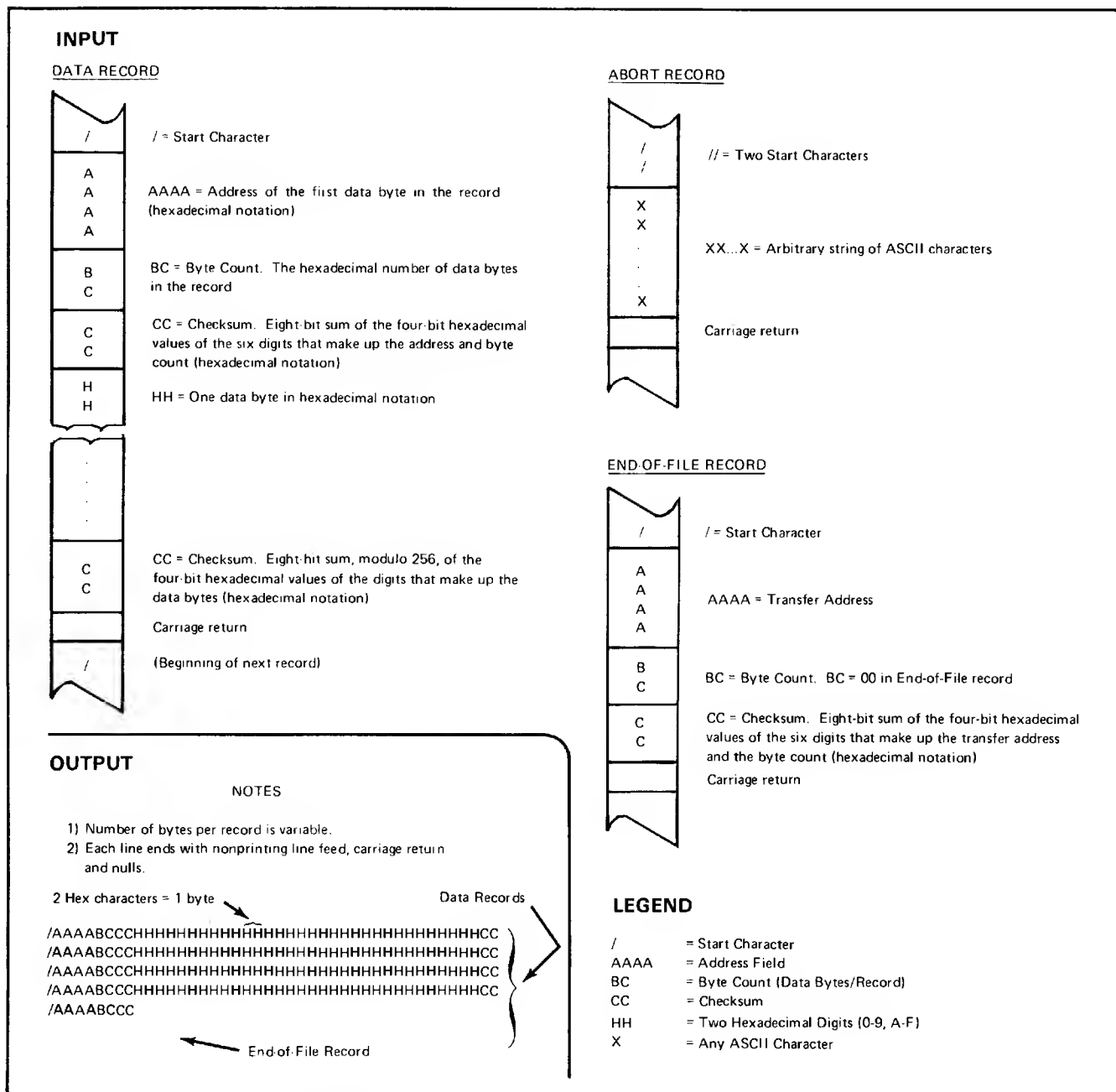


Figure A-14. Specifications for Tektronix Hexadecimal Data Files



• **HEWLETT-PACKARD 64000 ABSOLUTE FORMAT, CODE 89**

Hewlett-Packard Absolute is a binary format with control and data-checking characters. See figure A-16.

Data files begin with a Start-of-File record including the data bus width, data width base, transfer address, and a checksum of the bytes in the record.

Data records follow the Start-of-File record. Each begins with 2 byte counts: the first expresses the number of 16-bit words in the record not including the checksum and itself; the second expresses the number of 8-bit data bytes in the record. Next comes a 32-bit address which describes the storage location of the following data byte. Data bytes follow; after the last data byte comes a checksum of every byte in the record except the first byte.

The End-of-File record consists only of a byte count, which is always zero.

• **TEXAS INSTRUMENTS SDSMAC FORMAT, CODE 90**

Data files in the SDSMAC format consist of a Start-of-File record, data records, and an End-of-File record. See figure A-17.

Each record is composed of a series of small fields, each initiated by a tag character. The programmer recognizes and acknowledges the following tag characters:

- 0 - always followed by a file header.
- 7 - always followed by a checksum which the programmer acknowledges.
- 8 - always followed by a checksum which the programmer ignores.
- 9 - always followed by a load address.
- B - always followed by 4 data characters.
- F - denotes the end of a data record.

The Start-of-File record begins with a tag character and a 12-character file header. Next come interspersed address

fields and data fields (each with tag characters). If any data fields appear before the first address field in the file, the first of those data fields is assigned to address 0000. Address fields may be expressed for any data byte, but none are required. The record ends with a checksum field initiated by the tag character 7 or 8, a 4-character checksum, and the tag character F.

Data records follow the same format as the Start-of-File record but do not contain a file header.

The End-of-File record consists of a colon (:) only. The output translator sends a control S after the colon.

• **INTEL MCS-86 HEXADECIMAL OBJECT, CODE 88**

The Intel 16-Bit Hexadecimal Object file record format is basically the same as the Intel Intellec 8/MDS (Code 83). It starts with nine characters (four fields) that define the start of record, byte count, load address, and record type. It ends with a 2-character checksum. figure A-12 (Intel Intellec 8/MDS) illustrates this format.

There are four record types:

- 00 = data record
- 01 = end record (signals end of file)
- 02 = extended address record (added to the offset to determine the absolute destination address)
- 03 = start record (ignored)

Record type 02, the extended address record, defines bits 4 to 19 of the segment base address. It can appear randomly anywhere within the object file and in any order; *i.e.*, it can be defined such that the data bytes at high addresses are sent before the bytes at lower addresses. Because the data bytes are sent in nonsequential fashion, the address offset must be entered into the programmer every time the data transfer is initiated. It is the same as a data record with only four data digits. It's address field is always 0000.

**NOTE**

*Always specify the address offset when using this format, even when the offset is zero.*

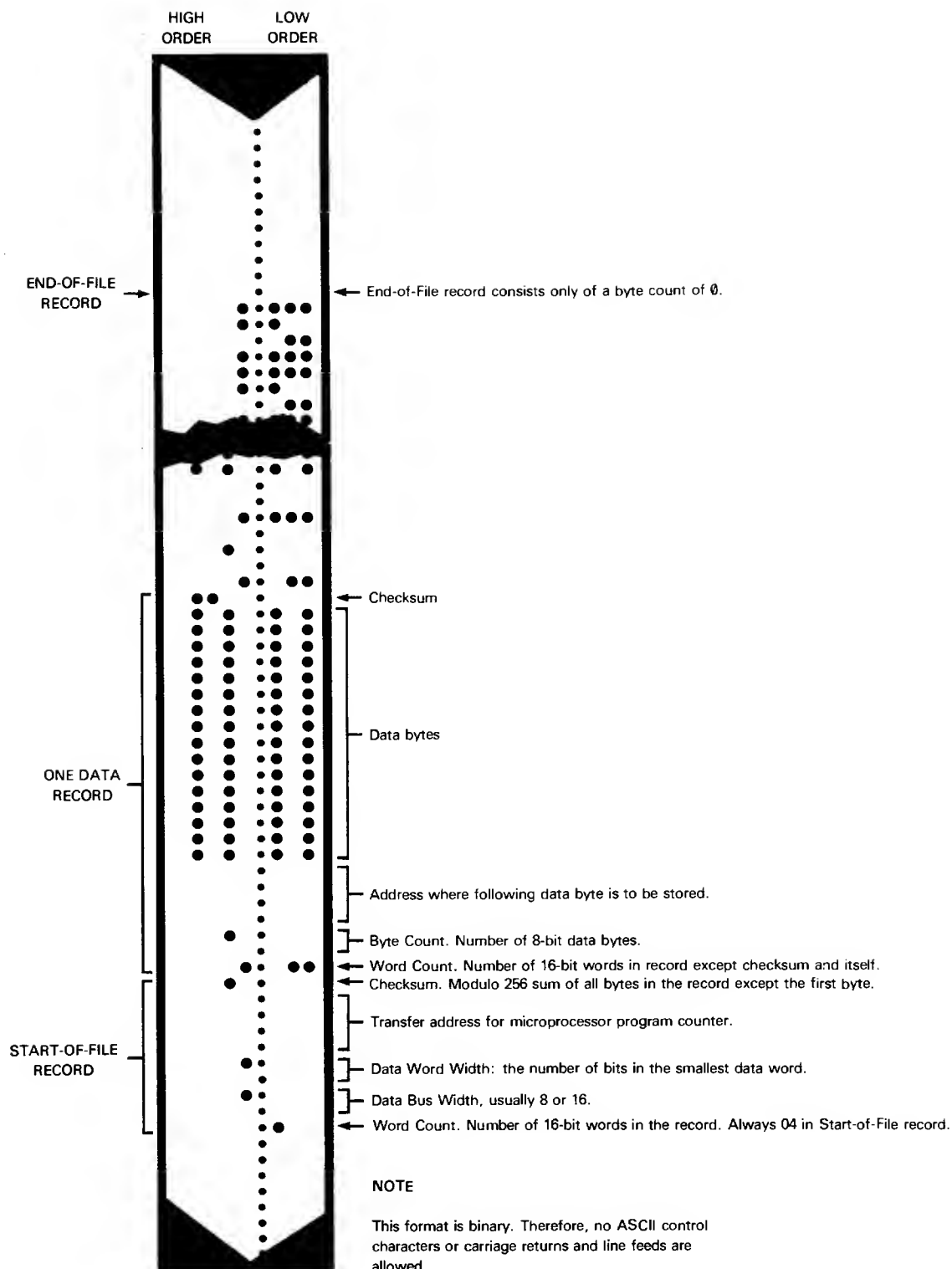
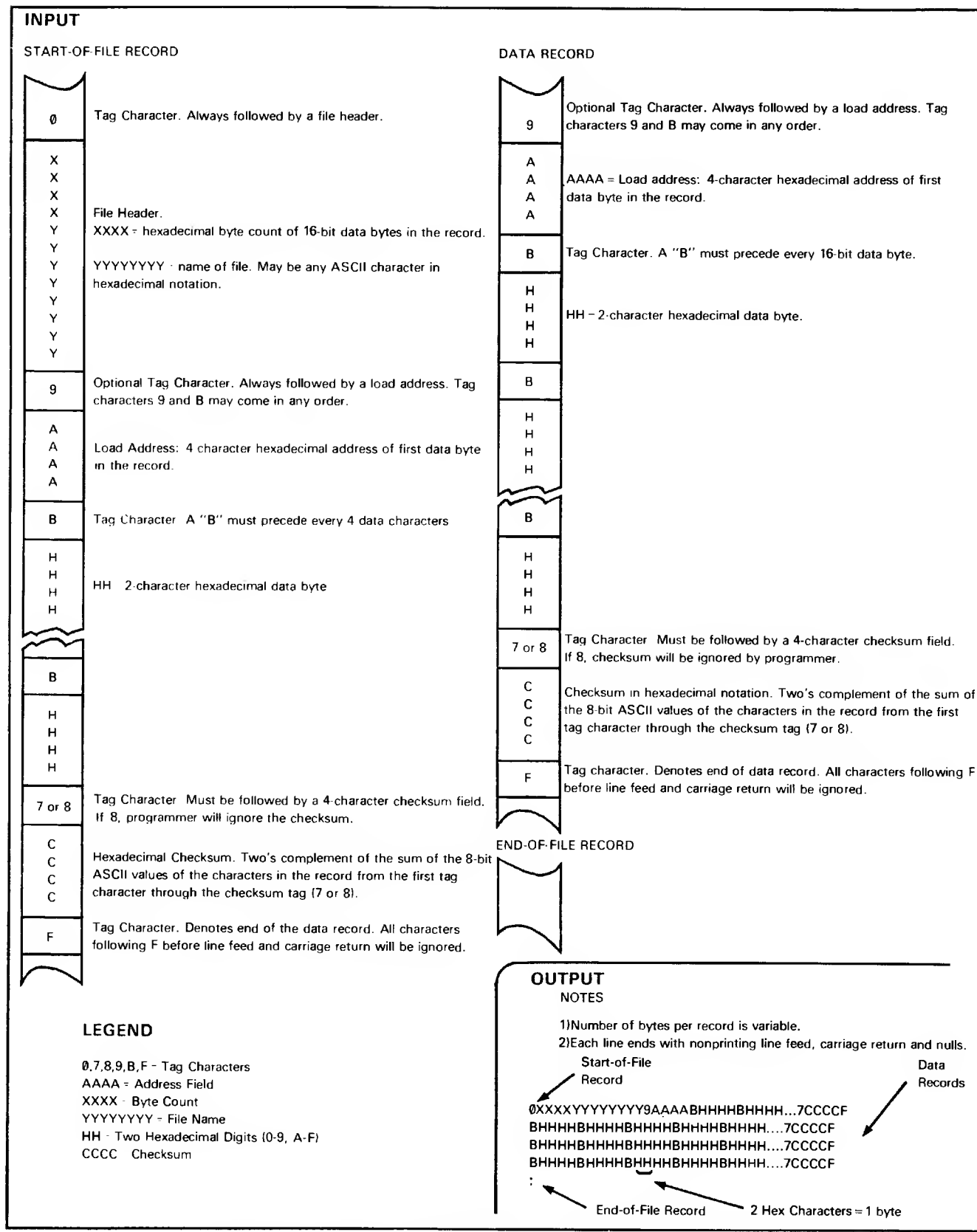


Figure A-16. Specifications for Hewlett Packard Absolute Format Data Files



## **APPENDIX B**

### **REFERENCE MATERIAL**

**Table B-1. Glossary**

**Table B-2. Abbreviations**

**Table B-3. Cross-Reference Chart of Number Bases**

**Table B-4. ASCII and IEEE Code Chart**

**Table B-5. ASCII Control Characters**

**Table B-1. Glossary**

**address field.** Optional set of control characters in a data translation format. It defines the address of the next data byte.

**address offset.** A 4-digit hex value subtracted from addresses on input and then added to addresses output from the programmer. The result is added to the begin device address or begin RAM address as applicable.

**begin device address.** The first device address from which or to which data is being transferred.

**begin RAM address.** The first address of the programmer data RAM from which or to which data is to be transferred.

**blank check.** A test performed by a programmer to detect the presence of any programmed bits. A device with no programmed bits is "blank."

**block size.** The hexadecimal number of bytes to be transferred in a data transfer.

**data translation format.** Form in which the translator software accepts input data. Also the form for data output by the unit.

**default value.** The value the unit uses for a parameter unless the operator specifies another value.

**device.** Any PROM, EPROM, MOS PROM, or EEPROM.

**end code.** Character in a data translation format which signals the completion of a data transfer.

**error code.** A code which signals specific errors to the operator.

**Family and Pinout Codes.** Two-digit codes used to identify programming variables including pinout, address limit and programming algorithms.

**FIP.** Flourescent Indicator Panel.

**handshaking.** The required sequence of signals for communication between two units. The I/O bus protocol for a unit defines its handshaking requirements. This is especially true for asynchronous I/O systems in which each signal requires a response to complete an I/O operation.

**illegal-bit test.** A test performed by a programmer to detect the presence of any programmed bits of incorrect polarity (illegal bits).

**mode.** A software routine in a machine, characterized by a specific automatic sequence of steps.

**nibble.** One half of an 8-bit byte.

**record size.** The number of bytes printed on a line of a teletype or other printer; or the number of bytes printed on a paper tape before another address field is printed.

**scratch pad memory.** The internal memory used for performing calculations.

**select function.** A 2-digit hex number used to specify data translation formats, serial interface operations, or certain RAM data manipulations.

**start code.** Character in a data translation format which signals the beginning of a data transfer.

**sum-check.** A summation of bits calculated according to the rules of simple addition and usually expressed as a 4-digit hex number; any carry from the most significant bit or digit is discarded. A sum-check is used to verify the integrity of data transfers.

HEX DATA	BINARY DATA
84	10000100
C1	11000001
62	01100010
24	00100100
<b>01CB</b>	<b>0000 0001 1100 1011</b>
Sum-check in hexadecimal notation	Sixteen-bit binary sum-check

**Figure B-1. Sample Sum-check Calculation**

**waveforms (programmable).** The graphical representation of the timing and magnitude of programming pulses. If the programming waveforms are not kept within tolerance, programming yield is jeopardized.

**word limit.** The highest address in a device. For example, the word limit of a 1Kx8 device is 1K (or hex 3FF). Synonymous with address limit.

**word width.** The number of bits in a byte or word (4 or 8).

**Table B-2. Abbreviations**

The following is a list of abbreviations commonly used in Data I/O Instruction manuals.

A <sub>4</sub> - address line 4	IRQ - Interrupt Request
ADDR - address	J - jack or connector
BC - Byte Count	JP - jumper
BR - bridge rectifier	K - relay
C - capacitor	LIM - limit
Clk - clock	LSB - Least Significant Bit
Clk. Inh. - clock inhibit	LSD - Least Significant Digit
Cntl. - control	MSB - Most Significant Bit
Cont. - control	MSD - Most Significant Digit
CR - diode	NMI - Non-Maskable Interrupt
CTS - Clear To Send	NO CONT SECT - No Contiguous Sector
D <sub>5</sub> - data line 5	Oper. - operate
DAC - Digital to Analog Converter	PA <sub>15</sub> - programmer address line 15
DC - Direct Current	PAK - programming module
DCD - Data Carrier Detect	PCS - Program Card Set
DCU - Data I/O Data Control Unit	PD <sub>6</sub> - programmer data line 6
DI <sub>2</sub> - data input 2	PN - Part Number
DIR - Directory	Prog - Program
DO <sub>2</sub> - data output 2	Prog. Pulse - Program Pulse
DS - display	PROM - Programmable Read Only Memory
DSR - Data Set Ready	Q - transistor
DTR - Data Terminal Ready	R - resistor
DVM - digital voltmeter	RAM - Random Access Memory
Emul - emulate	Read Inh. - Read Inhibit
ERR - error	Rec. - receive
ESC - escape	Rev. - reverse
F - fuse	RP - resistor pack
FC - Translation Format Code	RST - Reset
FFPP - Family Code (FF) and Pinout Code (PP)	R/W - Read/Write
FIP - Fluorescent Indicator Panel	RXD - Receive Data
FPGA - Field Programmable Gate Array	S - switch
FPLA - Field Programmable Logic Array	TOR - Turn On Reset
FPLS - Field Programmable Logic Sequencer	TXD - Transmit Data
FPRP - Field Programmable ROM Patch	U - integrated circuit device
PAL - Programmable Array Logic	V•02 - the "AND"-ing of the Valid Memory Address line and the phase 2 line
FRME - frame	VFY - verify
Fwd. - Forward	VMA - Valid Memory Address
Gnd. - Ground	VR - Voltage Regulator
HLT. - Halt	VREF - Voltage Reference
HV - high voltage	W/L - Word Limit
ID <sub>4</sub> - identification line 4	Write Inh. - Write Inhibit
I/O - Input/Output	



Table B-3. Cross-Reference Chart of Number Bases

Binary	Octal	Hexadecimal	Decimal	Standard Abbreviation
0000	0	0	0	
0001	1	1	1	
0010	2	2	2	
0011	3	3	3	
0100	4	4	4	
0101	5	5	5	
0110	6	6	6	
0111	7	7	7	
1000	10	8	8	
1001	11	9	9	
1010	12	A	10	
1011	13	B	11	
1100	14	C	12	
1101	15	D	13	
1110	16	E	14	
1111	17	F	15	
0001 0000	20	10	16	
0010 0000	40	20	32	
0100 0000	100	40	64	
1000 0000	200	80	128	
0001 0000 0000	400	100	256	
0010 0000 0000	1000	200	512	
0100 0000 0000	2000	400	1,024	1K
1000 0000 0000	4000	800	2,048	2K
1100 0000 0000	6000	C00	3,072	3K
0001 0000 0000 0000	10000	1000	4,096	4K
0001 0100 0000 0000	12000	1400	5,120	5K
0001 1000 0000 0000	14000	1800	6,144	6K
0001 1100 0000 0000	16000	1C00	7,168	7K
0010 0000 0000 0000	20000	2000	8,192	8K
0010 0100 0000 0000	22000	2400	9,216	9K
0010 1000 0000 0000	24000	2800	10,240	10K
0100 0000 0000 0000	40000	4000	16,384	16K
1000 0000 0000 0000	100000	8000	32,768	32K
0001 0000 0000 0000 0000	200000	10000	65,536	64K

Table B-4. ASCII & IEEE Code Chart

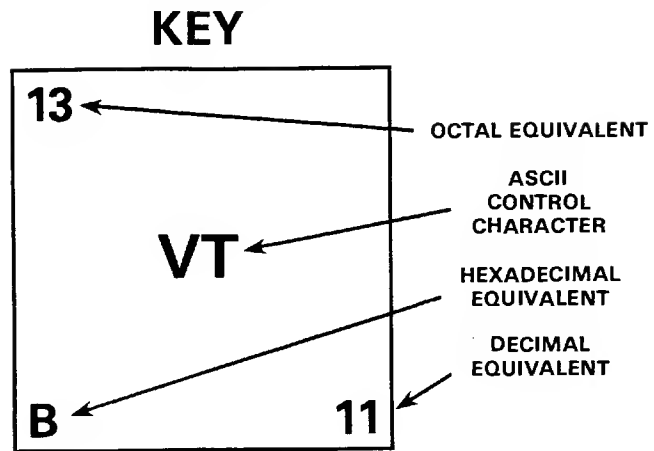


Table B-4. (con't.)

7 6 5  BITS 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS & SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 1 60 96	160 p 70 112
0 0 0 1	1 SOH 1	21 DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 EOT 4	24 DC4 14 20	44 \$ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 ENQ 5	25 NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 BS 8	30 CAN 18 24	50 ( 28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 HT 9	31 EM 19 25	51 ) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [ 5B 91	153 k 6B 107	173 } 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 V 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174   7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135 ] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 ? 3F 63	117 O 4F 79	137 _ 5F 95	157 o 6F 111	177 Rubout 7F 127
	Addressed Commands	Universal Commands	Listen Addresses		Talk Addresses		Secondary Addresses or Commands	

**Table B-5. ASCII Control Characters**

ACK	acknowledge
BEL	bell
BS	backspace
CAN	cancel
CR	carriage return
DC1	playback on, CNTL Q, X-ON
DC2	record on, CNTL R, PUNCH-ON, SOM
DC3	playback off, CNTL S, X-OFF
DC4	record off, CNTL T, PUNCH-OFF, EOM
DEL	delete, rubout
DLE	data link escape
EM	end of medium
ENQ	enquiry
EOT	end of transmission
ESC	escape
ETB	end of transmission block
ETX	end of text
FF	form feed
FS	file separator
GS	group separator
HT	horizontal tabulation
LF	line feed
NAK	negative acknowledge
NUL	null
RS	record separator
SI	shift in
SO	shift out
SOH	start of heading
STX	start of text
SUB	substitute
SYN	synchronous idle
US	unit separator
VT	vertical tab

# APPENDIX C

## COMPUTER REMOTE CONTROL

### C.1 INTRODUCTION

The Computer Remote Control is designed to allow complete control of the 22A by a computer. Linked directly to the programmer, the computer generates and sends commands to the programmer, determines variables for setting programming parameters (where needed), and reacts to information returned to it from the programmer.

While these commands may be sent by an operator at a terminal, the commands and syntax described in this manual were designed for ease of incorporation into a computer program. For use with a terminal, the standard Remote Control described in section 3 of this manual is more applicable.

### C.2 INSTALLATION

The 22A with Computer Remote Control must be connected to the computer according to RS232C specifications. The function of each serial port connector pin is described in section 2 of this manual. Refer to table 2-2 to determine the necessary connector pins for serial data transfers. The programmer's baud rate, parity, and stop bit settings are also described in section 2.

### C.3 OVERVIEW

Figure C-1 illustrates the basic components of the 22A under Computer Remote Control. Remote control commands are written into a computer's operating software, allowing it to control the 22A in much the same way as it would control any other peripheral such as a disc drive or printer.

Data transferred between the computer and programmer is generally in ASCII notation, encoded in the selected data translation format (see Appendix A), although straight binary transfer is also possible.

Commands are generated by the computer according to the computer's software or in response to keyboard entries. The computer sends commands to the 22A which executes the command (or tries to) and then sends back a response character.

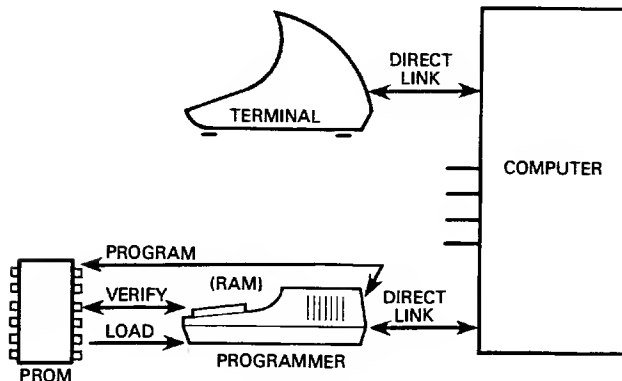


Figure C-1. Computer Remote Control Components

### C.4 RESPONSE CHARACTERS

The programmer sends a response character to the computer after every command. Table C-1 summarizes these.

Table C-1. Response Characters

CHARACTER	NAME	DESCRIPTION
>	Prompt	Sent on entering remote control, after an ESCAPE or BREAK key has halted a command, or after a command has been successfully executed. The programmer follows it with a carriage return.
F	Fail	Informs the computer that the programmer has failed to execute the last command entered. The programmer follows it with a carriage return.
?	Question	Informs the computer that the programmer does not understand a command or the command was invalid. The programmer follows it with a carriage return.

Whenever an error occurs, the 22A will send an F to the computer. The computer or the operator can respond by interrogating the programmer with the X or F command. The X command causes the programmer to send the computer a complete list of the error codes (described in section 3 of this manual) that have occurred. The F command codes all errors into a 32-bit error status word, as shown in figure C-2.

When a command is invalid or not understood by the programmer, it will send a ?. When this occurs, examine the last command entered to check its validity.

### C.5 ENTERING AND EXITING REMOTE CONTROL

To enter Computer Remote Control use Select Function F1. It is detailed in table 3-2 of this manual. While in Computer Remote Control the programmer display will show REMOTE MODE. On entering remote control, the programmer will retain all RAM data.

To exit Computer Remote Control via the 22A keyboard, press any of the four blue mode keys. To exit via the computer, use Z RETURN. The programmer will retain all RAM data and operating parameters except the address offset.

BIT NUMBER	VALUE	DESCRIPTION
31 30 29 28	8	<b>RECEIVE ERRORS</b> ANY ERROR. If the word contains any errors, the most significant bit (bit 31) will be high.
27 26 25 24	4 2 1	Serial-overflow error (42) Serial-framing error (41, 43) Buffer overflow, i.e., > 15 characters (48)
23 22 21 20	8 2	<b>PROGRAMMING ERRORS</b> Any device-related error L2 + L3 > Device
19 18 17 16	8 2 2 1	Device not blank (20) Illegal bit (21) Nonverify (23, 24, 29) Incomplete programming, (22, 25, 26, 30-39)
15 14 13 12	8 1	<b>I/O ERRORS</b> I/O error (46, 67, 84, 91-94, 95 or any I/O error) Compare error (52)
11 10 9 8	8 4 2 1	Sum-check error (82) Record-count error, MOS technology (93) Address-check error, Signetics and Tex Hex (92) Record-type error, Intel Intellec 8/MDS (94) Address error, i.e., > word limit (27) Data no hexadecimal (84, 86, 91)
7 6 5 4	8 2 1	<b>RAM ERRORS</b> RAM-hardware error (64, 66 or any RAM error) L2 + L3 > RAM (in RAM-RAM block move) Invalid center point for split or shuffle
3 2 1 0	8 2	Illegal split or shuffle RAM write error, or program-memory failure (63)

**EXAMPLE:**

What errors are indicated in this error status word: 80C80081?

8— the word contains error information

0— no receive errors

A— (= 8 + 2): 8 = Device-related error  
2 = L1 + L2 > RAM

8— device is not blank (error 20)

0— no input errors

0— no input errors

8— RAM error (error 62, and possible 64 and 66)

1— RAM write error

**NOTES**

- The numbers in parentheses are 22A error codes, defined in section 3.
- An error can cause as many as 3 bits to be high: the bit which represents the error, the most significant bit of the 8 bit-word in which the error bit occurs, and bit 31.
- After being read, the error-status word resets to zeros.

Figure C-2. Error-Status Word

## C.6 COMMAND SUMMARY

Table C-2 is a summary of Computer Remote Control commands. Figure C-3 is a flowchart of the command

protocol. Section C.7 gives further detailed descriptions of the command groups and individual commands.

Table C-2. Command Summary

COMMAND	NAME	DESCRIPTION	RESPONSE	NOTES
<b>CONTROL COMMANDS</b>				
	RETURN	Execute a command.		1,2
	ESC	Aborts a command.	>CRLF	1,2
	BREAK	Aborts a binary transfer.	>CRLF	1,2
<b>UTILITY COMMANDS</b>				
G	Software-configuration	This command sends a 4-digit hex number (XXXX) representing the software revision level in the programmer.	XXXX>CRLF	1,2
HHHH<	Set Begin RAM Address	Defines first RAM address to be used for data transfers. Also functions as the RAM Source Address in RAM-RAM Block Move. The default value is 0.	>CRLF	1,2
HHHH ;	Set Block Size	Sets number of bytes to be transferred. The default value is the device size, for device-related operations; RAM limit less the Begin RAM Address for I/O operations; no default for RAM-RAM Block Move.	>CRLF	1,2
HHHH :	Set Begin Device Address	Sets the first device address to be used in data transfers. Also functions as the RAM-destination address in RAM-RAM Block Move. The default value is 0.	>CRLF	1,2
HH ]	Select Function	This command accesses various functions available from front panel control. These Select functions include: CC Display Family and Pinout Code (DSP FAM/PIN) CD View I.D. CE Normal Reject CF One Pulse Reject A4 Clear All RAM F4 Nibble Mode F5 Binary Base F6 Octal Base F7 Hex Base F8 Byte/Nibble Mode FE Power Down Save	>CRLF	1,2
S	Sum-check	Causes programmer to calculate the sum-check of RAM data.	XXXX>CRLF	1,2
F	Error-Status Inquiry	Programmer returns a 32-bit word that codes errors accumulated. Error-status word resets to zeros after interrogation. (Error-status word is shown in figure C-2.)	XXXXXXXX>CRLF (See figure C-2)	1,2

Table C-2. Command Summary (continued)

COMMAND	NAME	DESCRIPTION	RESPONSE	NOTES
X	Error-Code Inquiry	Programmer outputs the error codes stored in scratch-RAM and then clears them from memory. Refer to the error list in section 3.	XXXX>CRLF	1,2
H	No Operation	This is a null command and always returns a prompt character (>).	>CRLF	1,2
Z	Escape Remote Control	Return control to the programmer.	None	
<b>DEVICE COMMANDS</b>				
T	Illegal-Bit Test	Test for illegal bit in device.	>CRLF	1,2
B	Blank Check	Check that no bits are programmed in device.	>CRLF	1,2
[	Family and Pinout Inquiry	Programmer sends a 4-digit number (FFPP) where FF is the Family Code and PP is the Pinout Code in effect.	FFPP>CRLF	1,2
FFPP @	Select Family and Pinout	A 2-digit Family Code (FF) and a 2-digit Pinout Code (PP) set up the particular device for device-related operations.	>CRLF	1,2
R	Respond	Programmer indicates status determined by device selected and outputs AAA/B/C or AAAA/B/C, where AAA or AAAA = device word limit, B = byte size and C = VOL/VOH status (1 = VOL; 0 = VOH).	AAA/B/C>CRLF	1,2
L	Load	Load device data into RAM.	>CRLF	1,2
P	Program	Program RAM data into device.	>CRLF	1,2
V	Verify	Verify device against RAM.	>CRLF	1,2
<b>I/O COMMANDS</b>				
D	Select Odd Parity	Sets odd parity for input and output data.	>CRLF	1,2
E	Select Even Parity	Sets even parity for input and output data.	>CRLF	1,2
N	Select No Parity	Sets no parity for input and output data.	>CRLF	1,2
J	Set 1 Stop Bit	Sets 1 stop bit for input and output data.	>CRLF	1,2
K	Set 2 Stop Bits	Sets 2 stop bits for input and output data.	>CRLF	1,2



Table C-2. Command Summary (continued)

COMMAND	NAME	DESCRIPTION	RESPONSE	NOTES
FC A	Select Translation Format	Two Characters (FC) before A define the data translation format for I/O data transfer. The default value is MOS Technology Format, #81.	>CRLF	1,2
HH M	Select Record Size	Two hex characters before M define output record size. The default value is 16 bytes per record (8 bytes per record in Fairchild Fairbug).	>CRLF	1,2
HH U	Set Nulls	Two hex characters before U set the number of nulls output after carriage returns and enables line feeds. The default value is no nulls and no line feeds.	>CRLF	1,2
HHHH W	Set Address Offset	Up to eight hex characters before W define the offset added on output and subtracted on input. The default value is 0 (output) or first incoming address (input).	>CRLF	1,2
=	Disable Timeout	Disables the 25-second I/O timeout. Restored only at power on.	>CRLF	1,2
I	Input	Input data from computer to RAM.	>CRLF	1,2,3
O	Output	Output data from RAM to computer.	>CRLF	1,2,3
C	Compare	Compare RAM data with data input from computer.	>CRLF	1,2,3
Y	Parity-Error Inquiry	Responds with the hex number of parity errors since last Y command, since power on, or since last parity command (D, E, or N).	XXXX >CRLF	1,2
<b>EDITING COMMANDS</b>				
Q	Swap Nibbles	Exchanges high- and low-order halves of every word in RAM.	>CRLF	1,2
\	RAM-RAM Block Move	Initiates data transfer from one RAM location to another. The Begin RAM Address, block size, and Begin Device Address must be set first.	>CRLF	1,2
HHHH ?	Split RAM Data	For 16-bit microprocessor data. Splits even- and odd-numbered bytes into two blocks separated by a center point, HHHH, which must be a power of 2 between 0 and RAM midpoint. The default value is the RAM midpoint.	>CRLF	1,2
HHHH >	Shuffle RAM Data	For 16-bit microprocessor data. Merges block above center point HHHH with block below. Center point must be a power of 2 between 0 and RAM midpoint. The default value is the RAM midpoint.	>CRLF	1,2
Λ	Clear All RAM	Clears all of the 22A's data RAM to zeros.	>CRLF	1,2

**NOTES**

1. LF=Line Feed, CR=carriage return  
 . Line Feeds are present only if the null command (U) has been sent.

3. Response occurs at end of data transmission with proper termination.

## C.7 COMMAND GROUPS

This section gives detailed descriptions and usage of the command groups and individual commands used in Computer Remote Control.

### C.7.1 CONTROL COMMANDS

These commands are used to execute or suspend a command.

**RETURN.** Carriage return character which executes each command. It must be sent to the programmer immediately after the command. All commands are ignored if not followed by a RETURN.

**ESCAPE or BREAK.** These commands cause the programmer to unconditionally halt (abort) any operation in progress, output a >, and await further instructions from the computer. Do not transmit an Escape or Break command when edit commands are being executed.

### C.7.2 UTILITY COMMANDS

These commands set or check various operating parameters related to operations.

---

#### SOFTWARE CONFIGURATION NUMBER

**G RETURN**

On command, the programmer sends the 4-digit hex number representing the particular configuration or revision level of software resident in the 22A.

---

#### SET BEGIN RAM ADDRESS

**HHHH < RETURN**

This command, preceded by a 4-digit hex address (HHHH), defines the first RAM address to be used for data transfers. It is also the RAM source address when used in a Block Move. Setting the Begin RAM Address clears any previously entered Block Size. The default value is 0.

---

#### SET BLOCK SIZE

**HHHH ; RETURN**

Sets the hex number of bytes (HHHH) to be transferred. The default value is the programming module word limit for device-related operations or the RAM limit less the Begin RAM Address for I/O operations; there is no default for Block Moves.

---

#### SET BEGIN DEVICE ADDRESS

**HHHH : RETURN**

This command, preceded by a 4-digit hex address (HHHH), defines the first device address to be used for data transfers. It is also used as the RAM destination address when used in a Block Move. The default value is 0.

---

#### SELECT FUNCTION

**HH ] RETURN**

Allows entry of some select functions. See section C.6 for a complete list.

---

#### SUM-CHECK

**S RETURN**

This command instructs the programmer to calculate the 4-digit hex sum-check of RAM from 0 (or begin RAM point) to RAM word limit, device word limit, or the limit defined by the ; command, whichever is smaller. Sum-check is defined in the Glossary in Appendix B.

---

#### ERROR-STATUS INQUIRY

**F RETURN**

On this command, the programmer returns a 32-bit word, displayed as 8 hex characters, that codes errors accumulated. The error-status word resets to all zeros after interrogation. See figure C-2.

---

#### ERROR CODE INQUIRY

**X RETURN**

The programmer responds to this command with hex error codes previously stored. After execution, the error codes are cleared from memory. Section 3 of this manual lists and describes all the error codes.

---

#### NO OPERATION

**H RETURN**

This is a null command and always returns a prompt (>).

---

#### ESCAPE REMOTE CONTROL

**Z RETURN**

This command returns control to the 22A keyboard. All RAM data and operating parameters except the address offset are retained.

### C.7.3 DEVICE COMMANDS

This group of commands executes the operations used in device programming. Figure C-3 illustrates their respective protocols.

#### NOTE

*Illegal-Bit Test, Blank Check, Load, Program, and Verify are performed from the Begin RAM Address to the device word limit, RAM word limit or Block Size, whichever is smaller.*

---

**ILLEGAL-BIT TEST****T RETURN**

Instructs the programmer to perform an illegal-bit test and stores the error code and returns an F if an illegal-bit occurs (programmed device bit whose corresponding RAM bit is unprogrammed).

---

**BLANK CHECK****B RETURN**

Instructs the programmer to do a blank check (search the device for programmed bits) and store the error code and return an F if the device is nonblank.

---

**FAMILY AND PINOUT INQUIRY****I RETURN**

The 22A responds to this command with the Family and Pinout Codes of the selected device.

---

**SELECT FAMILY AND PINOUT****FFPP @ RETURN**

Selects a 2-digit Family Code (FF) and a 2-digit Pinout Code (PP).

---

**RESPOND****R RETURN**

The programmer checks the device type selected and outputs:

AAAA / B / C  
device word limit  
byte size  
VOL (1) or VOH (0)

---

**LOAD****L RETURN**

This command instructs the programmer to load data into RAM from the device within the parameters defined by the Begin RAM Address, Block Size, and Begin Device Address.

---

**PROGRAM****P RETURN**

This command instructs the programmer to program the data in RAM into the device within the parameters defined by the Begin RAM Address, Block Size, and Begin Device Address.

---

**VERIFY****V RETURN**

This command instructs the programmer to compare RAM data with the data of the device within the parameters defined by the Begin RAM Address, Block Size, and Begin Device Address.

**C.7.4 I/O COMMANDS**

This group of commands sets up the 22A to transmit or receive data through the serial port. This includes inputting or outputting data, selecting a data translation format, setting parity, address controls, and other considerations incidental to I/O data transfers.

---

**SELECT ODD PARITY****D RETURN**

Instructs the programmer to set odd parity for output data and inspect incoming data for odd parity.

---

**SELECT EVEN PARITY****E RETURN**

This command instructs the programmer to set even parity for output data and inspect incoming data for even parity.

---

**SELECT NO PARITY****N RETURN**

This command instructs the programmer to not check incoming data for parity, and to output data without parity.

---

**SET 1 STOP BIT****J RETURN**

On receiving this command, the programmer sets one stop bit for serial data transfers.

---

**SET 2 STOP BITS****K RETURN**

On receiving this command, the programmer sets two stop bits for serial data transfers.

---

**SET TRANSLATION  
FORMAT****FC A RETURN**

This command selects the input or output data translation format expressed by the format code (FC) in the command. Table C-3 lists the format codes. The default value is MOS Technology Format, #81. All the data translation formats available are detailed in Appendix A of this manual.

**Table C-3. Data Translation Formats**

<b>FORMAT</b>	<b>CODE</b>
Binary	10
DEC Binary	11
ASCII-BNPF	01 (05) *
ASCII-BHLF	02 (06) *
ASCII-B10F	03 (07) *
5-level BNPF	08 (09) *
Spectrum	12 (13) *
ASCII-Octal (Space)	30 (35) +
ASCII-Octal (Percent)	31 (36) +
ASCII-Octal (Apostrophe)	32
ASCII-Octal SMS	37
ASCII-Hex (Space)	50 (55) +
ASCII-Hex (Percent)	51 (56) +
ASCII-Hex (Apostrophe)	52
ASCII-Hex SMS	57
ASCII-Hex (Comma)	53 (58) +
RCA Cosmac	70
Fairchild Fairbug	80
MOS Technology	81
Motorola Exorciser	82
Intel Intellec 8/MDS	83
Signetics Absolute Object	85
Tektronix Hexadecimal	86
Motorola Exormax	87
Intel MCS-86 Hexadecimal Object	88
Hewlett-Packard Absolute	89
Texas Instruments SDSMAC	90
<p>* For transmission of data without start codes, these alternate data translation format codes are used.</p> <p>+ For transmission of data without the SOH (CTRL A) start code, these alternate data translation format codes are used.</p>	

#### **SELECT RECORD SIZE**

**HH M RETURN**

The 2 hex characters (HH) before M define the number of data bytes per record in serial-output operations. The default value is 16 bytes per record for data translation formats with a variable record size (all formats except ASCII-Binary, Spectrum and Fairchild Fairbug).

#### **CLEAR ALL RAM**

**^ RETURN**

Clears all of the 22A data RAM to zeros.

#### **SET NULLS**

**HH U RETURN**

The 2 hex characters (HH) before U set the number of nulls to be output following the carriage return in serial-output operations, and enable line feeds. The default value is no nulls or line feeds. Entering FF before U will also invoke the default value.

#### **DISABLE TIMEOUT**

**= RETURN**

This command disables the 25-second I/O timeout.

#### **INPUT DATA**

**I RETURN**

This command instructs the programmer to accept formatted data from the computer.

#### **OUTPUT DATA**

**O RETURN**

This command instructs the programmer to translate RAM data into the selected data translation format and output this data to the computer. The programmer will stop outputting on receipt of the X-OFF character, DC-3 (Control S), and will resume on receipt of the X-ON character, DC-1 (Control Q).

#### **COMPARE DATA**

**C RETURN**

This command instructs the programmer to compare data in RAM with data input from the computer.

#### **PARITY-ERROR INQUIRY**

**Y RETURN**

This command instructs the programmer to output the hex number of parity errors (up to FFF) encountered since power-on, since the last Y command, or since the last parity command (D, E, or N).

### **C.7.5 EDITING COMMANDS**

This group of commands is used for manipulating data in the 22A data RAM.

#### **SWAP NIBBLES**

**Q RETURN**

Instructs the programmer to exchange high- and low-order halves of every word in RAM. This is useful when programming 4-bit devices with only one-half of RAM at a time.

---

**RAM-RAM BLOCK MOVE****\ RETURN**

This command moves a specified number of bytes (as specified by the Block Size) from one RAM location (as specified by the Begin RAM Address) to another (specified with the Begin Device Address Command).

---

**SPLIT RAM DATA****HHHH ? RETURN**

For 16-bit microprocessor data; complement of Shuffle RAM Data (below). After a block of data is input or loaded to RAM (each sequential pair of 8-bit bytes representing a 16-bit word), the command "splits" the block into two adjacent blocks, separated by the specified center point (HHHH). The split stores the even-numbered 8-bit bytes of each byte pair in sequence from address 0 to the center point; odd-numbered bytes are stored in sequence at addresses beginning at the center point. The reorganized data occupies the same original block in RAM.

Each block of data can then be programmed into an 8-bit device, and the 2 devices can be addressed in parallel (while in use) to deliver 16-bit words to the processor.

Typically, the center point will equal the number of words in the 8-bit device to be programmed. In any event, it must meet two requirements:

1. It must be a power of 2.
2. It must be less than or equal to half the size of the resident RAM.

The center-point default value is the RAM midpoint.

---

**SHUFFLE RAM DATA****HHHH > RETURN**

For 16-bit microprocessor data. Complement of Split RAM Data, this command merges into one block the two adjacent blocks of data which meet at the specified center point address (HHHH). Two 8-bit devices are first loaded adjacent to each other in RAM, beginning at address 0, to create the two blocks, which are then merged for serial transfer. The center point must be a power of 2 between 0 and RAM midpoint. The center-point default value is the RAM midpoint.

---

**ADDRESS OFFSET****HHHH W RETURN**

This command specifies the value to be subtracted from addresses on input and added to them on output. Up to eight characters (in some formats) can be input before this command.

Figure C-3. Computer Remote Control

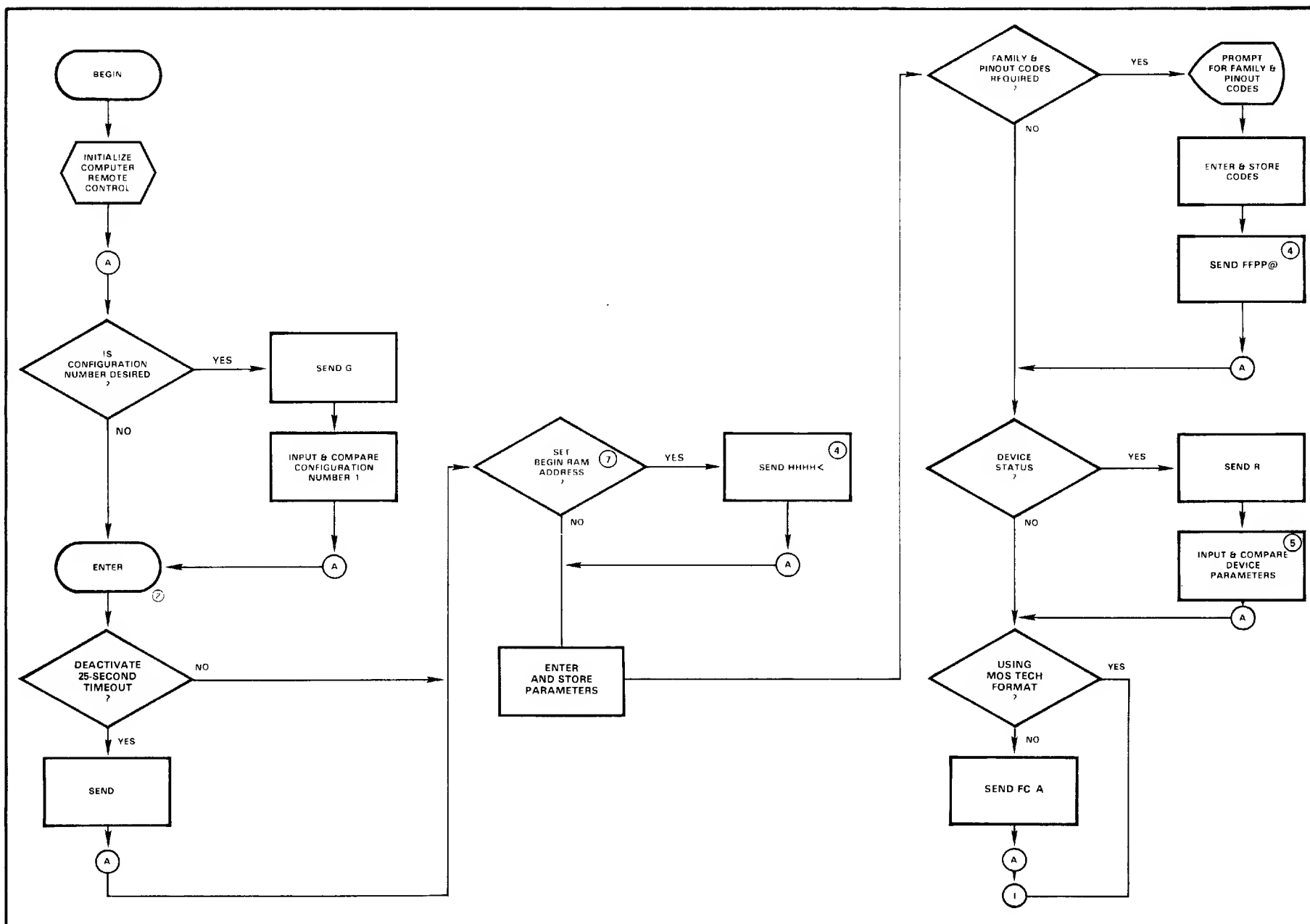
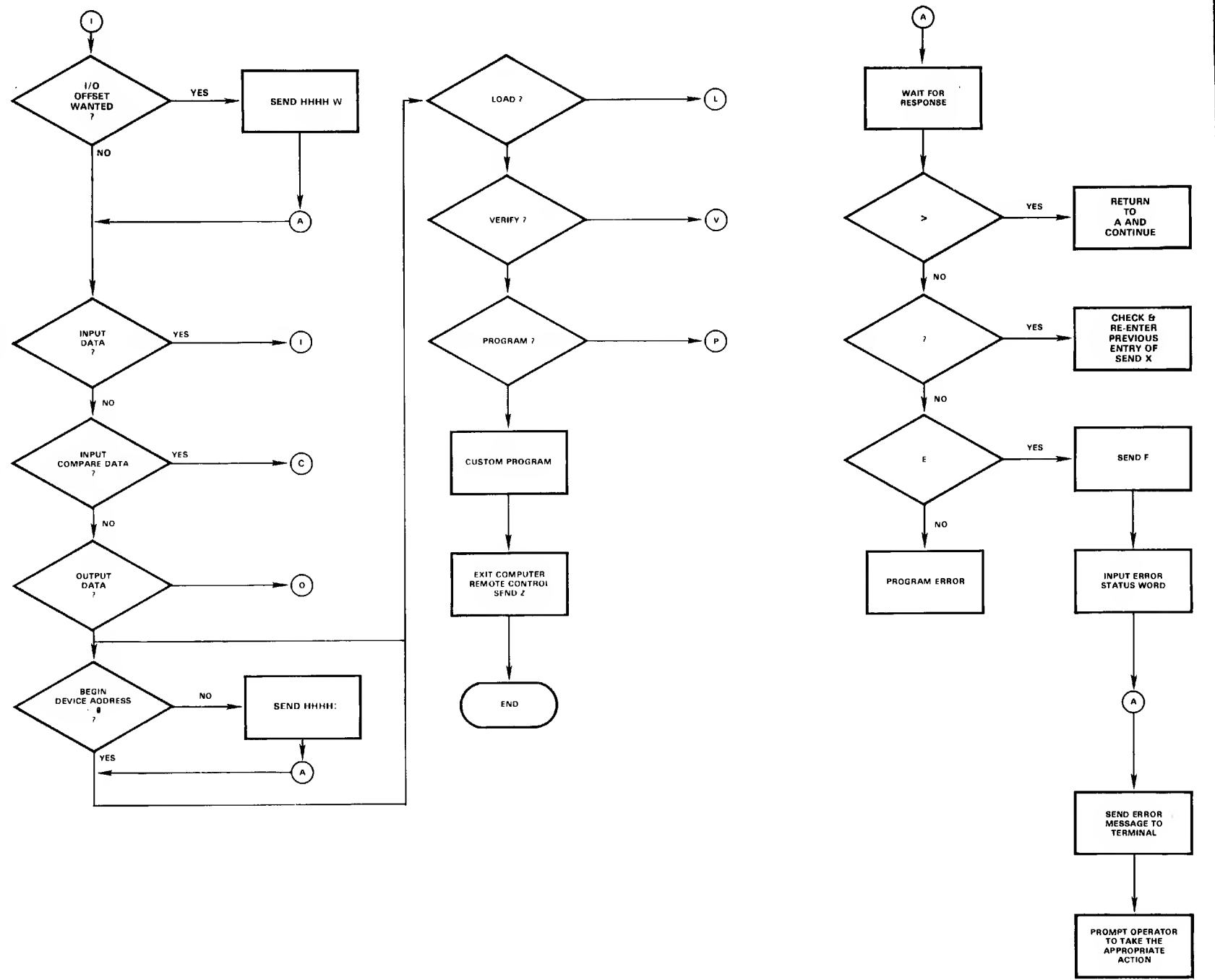


Figure C-3. Computer Remote Control (continued)



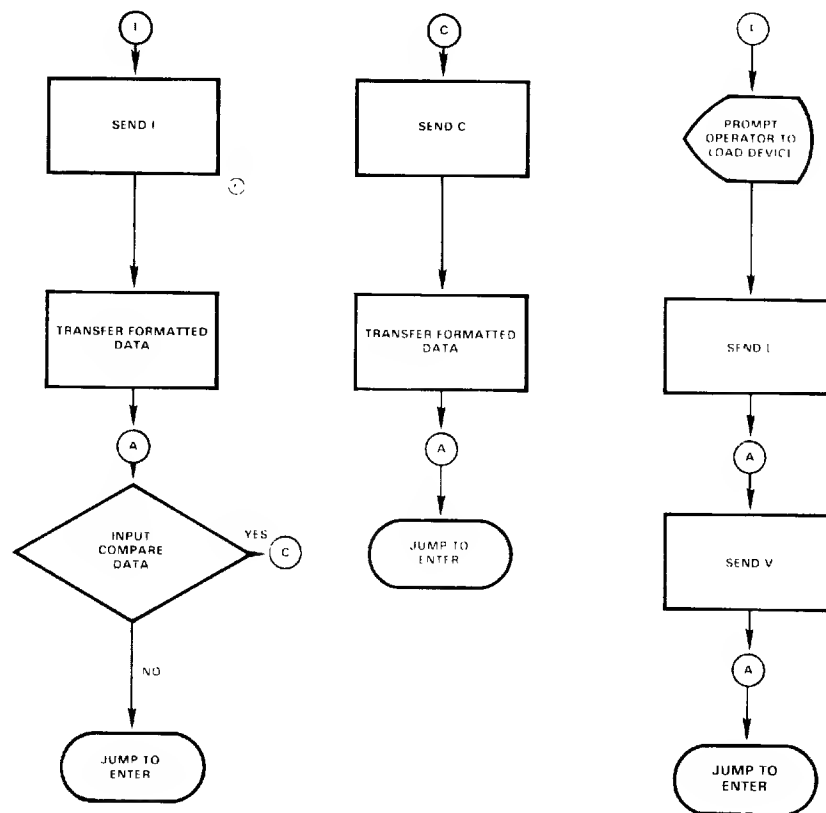


Figure C-3. Computer Remote Control (continued)



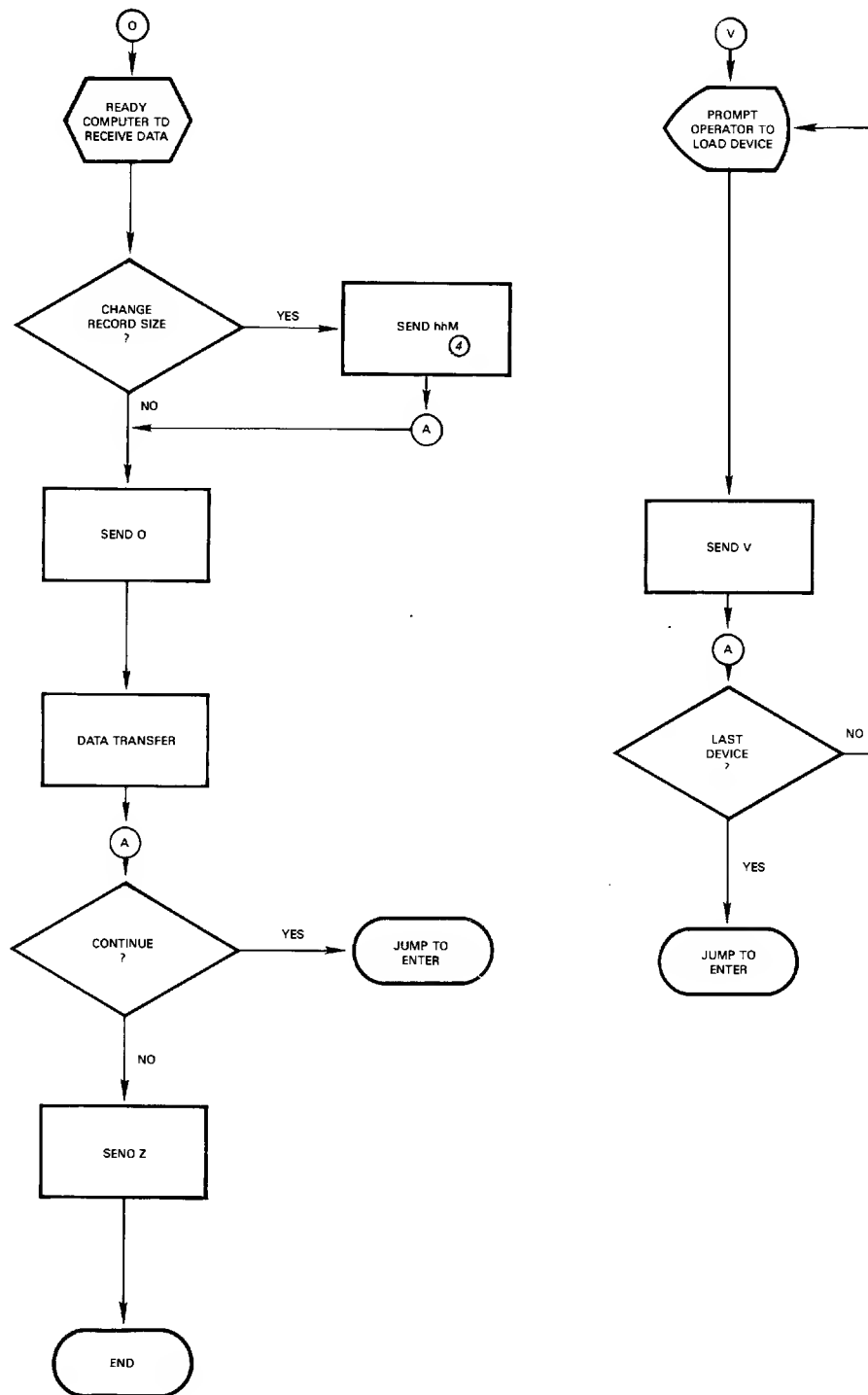
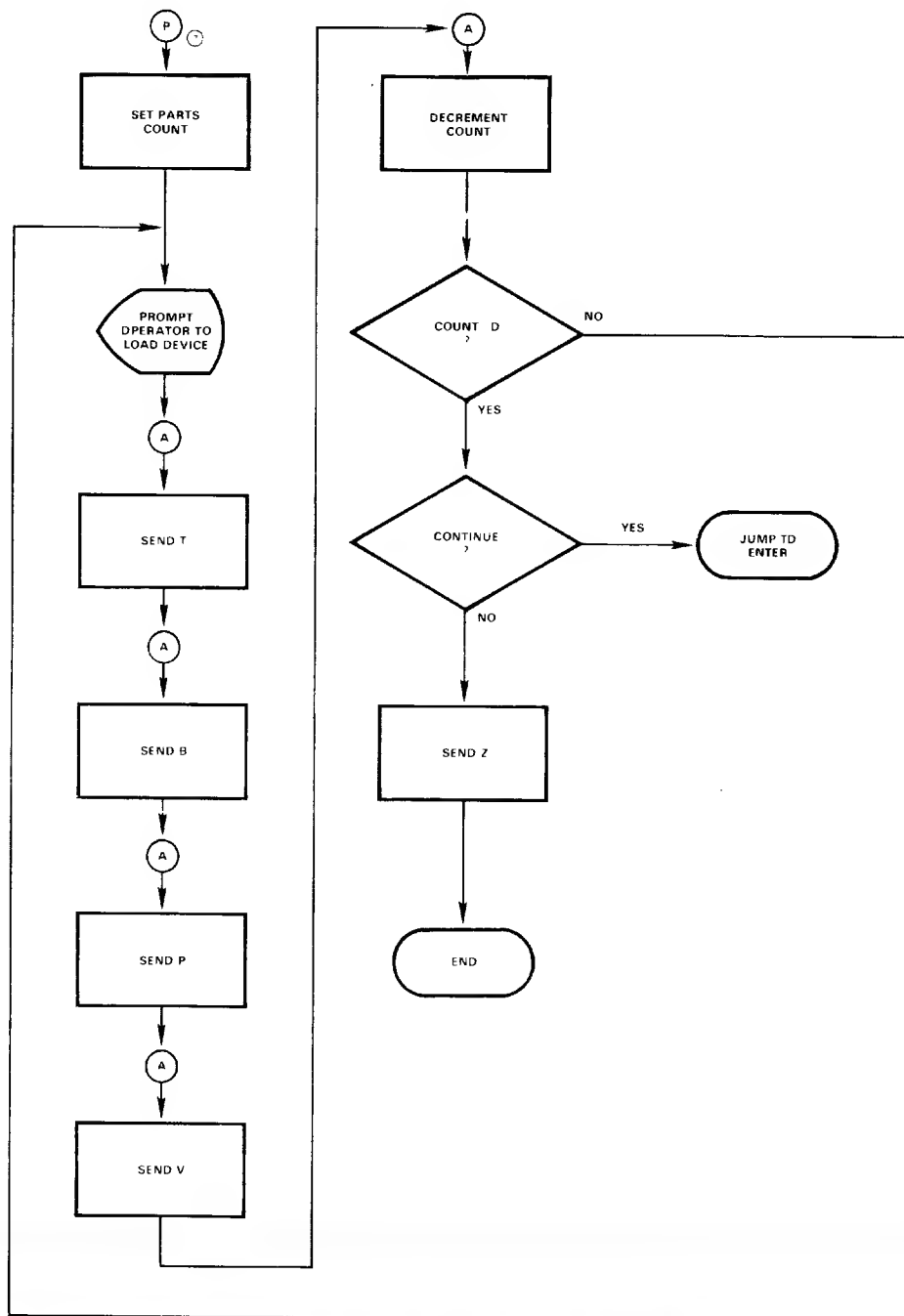


Figure C-3. Optional Computer Remote Control (continued)



**Figure C-3. Computer Remote Control (continued)**

#### NOTES

1. The configuration number command allows the program to query the programmer as to which version of remote control it is using.

2. The following commands can be invoked at any time in the sequence:

S Sum-check  
X Error Code Inquiry  
H No Operation

Each must be followed by a carriage return.

3. The default value is zero nulls. By entering a number of nulls, a line feed will accompany the carriage return.

4. The letters hhhh, hh, FFPP, and FC are used to denote variables that must be entered at this time.

5. Device parameters are output in the following format:

XXXX | Y | Z  
word limit word size (4 or 8) VOH or VOL (0 = VOH; 1 = VOL)

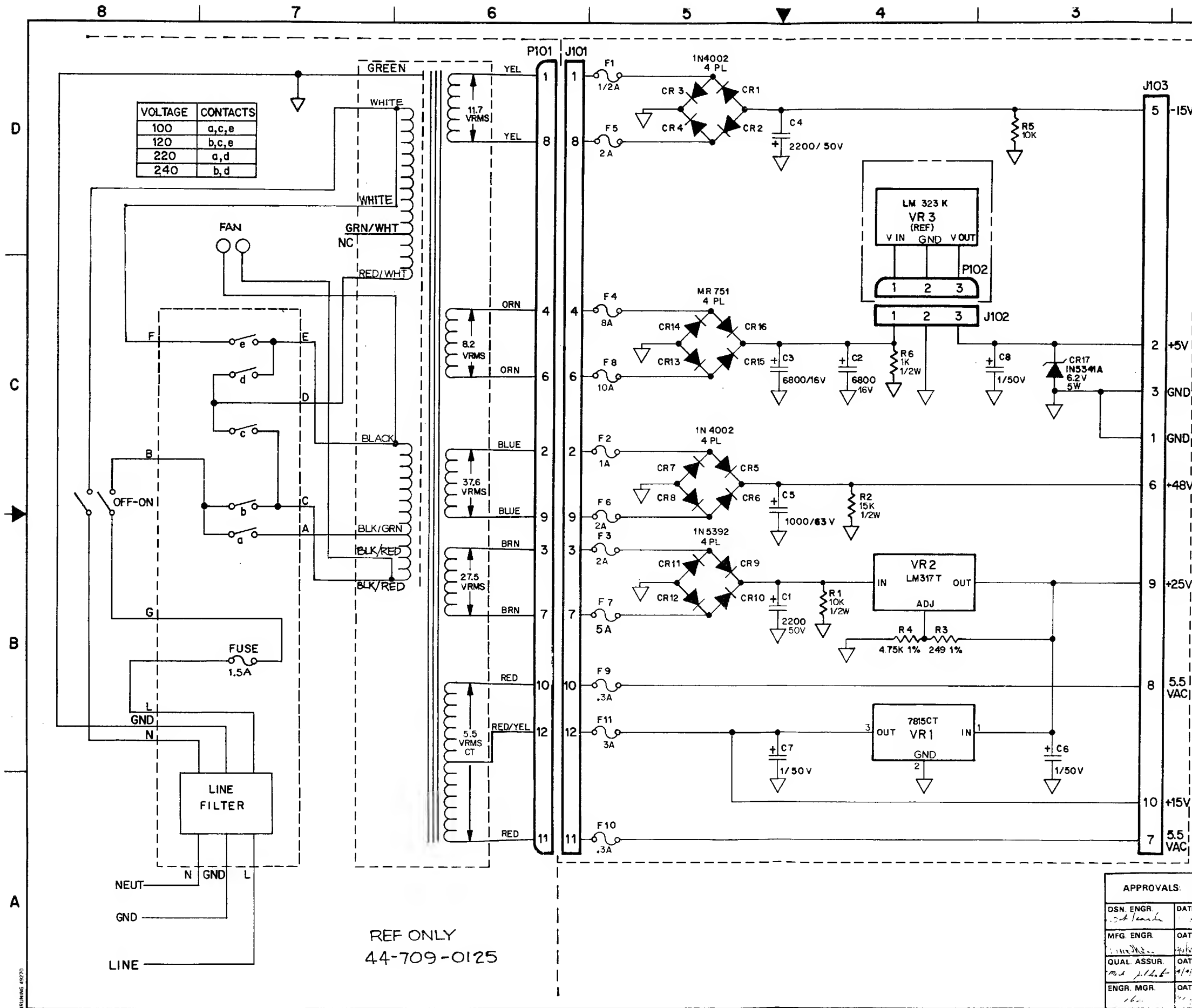
6. A 500 ms delay is advised in some cases.

7. To clear Begin RAM send < without a prefix.

## APPENDIX D

# SCHEMATICS

30-702-1774	Power Supply
30-702-1775	Controller
30-702-1773	Keyboard/Display
30-702-1770	Waveform Generator



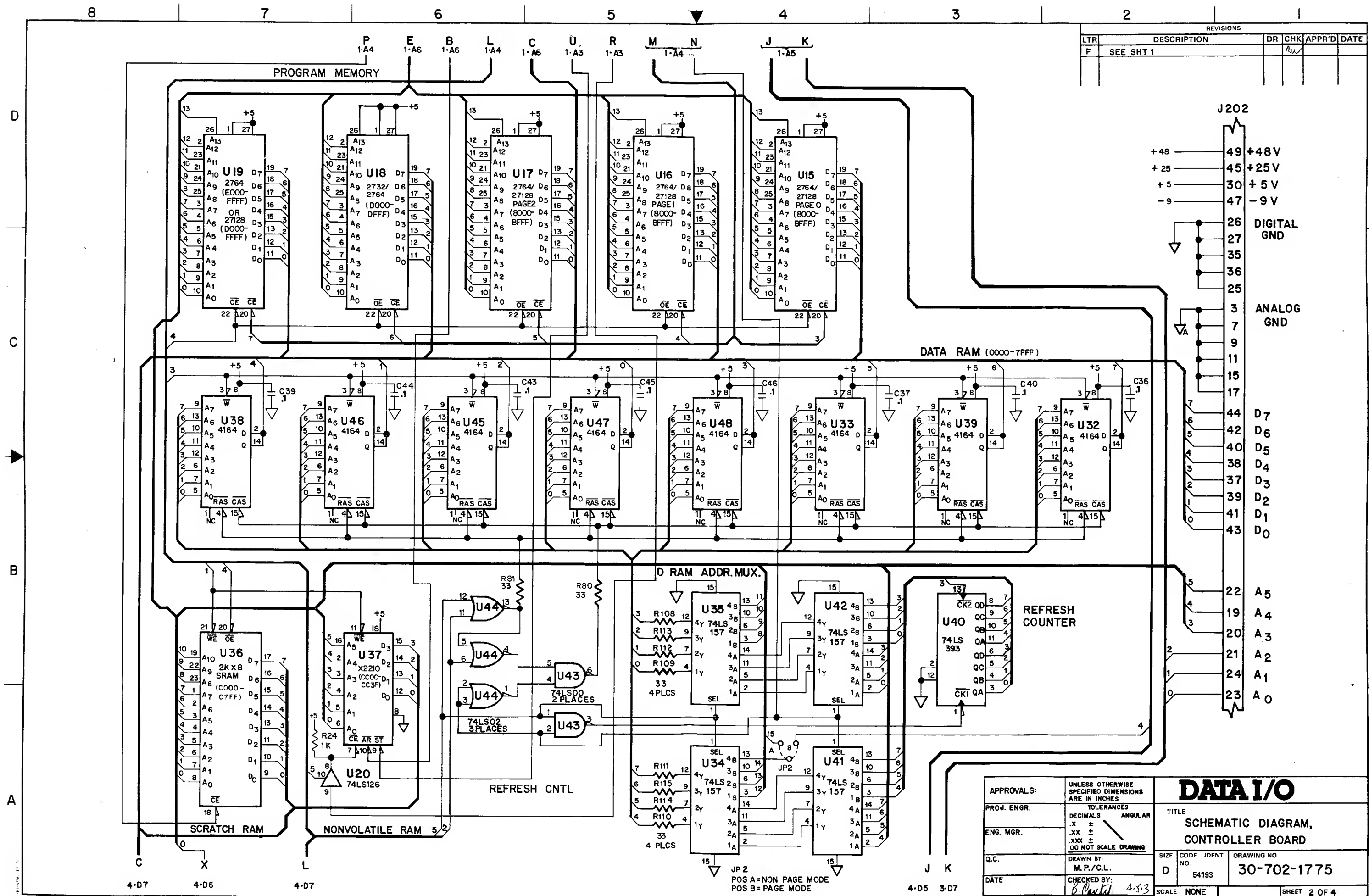
REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
A	RELEASE			4/83
B	ECN 4886	BV	7/01	
C	ECN 4944	SH		
D	INCORPORATION PER ECP0009	B.C.		

NOTES: UNLESS OTHERWISE SPECIFIED  
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5% .  
2. ALL CAPACITORS ARE IN MICROFARADS.  
3. LAST REFERENCE DESIGNATOR USED: C8, CR17, F11, J103, R6, VR2

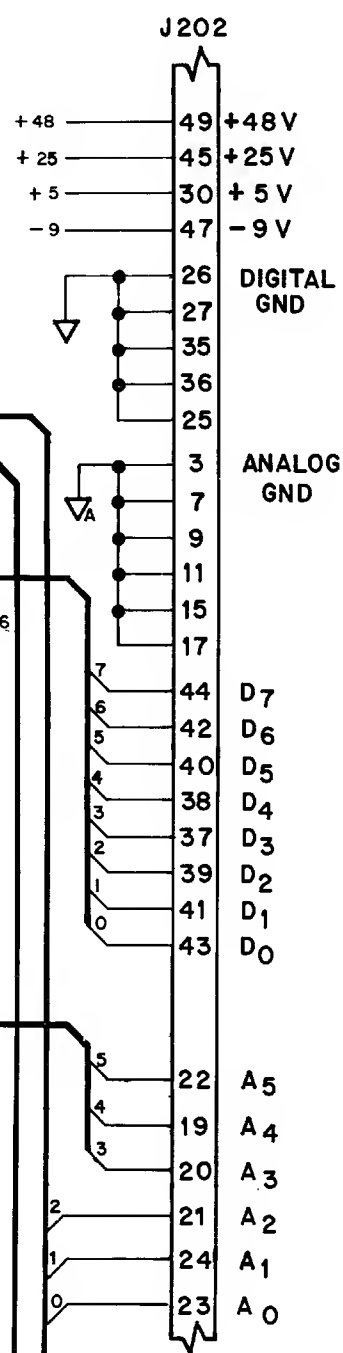
702-1774-001

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.		TOLERANCES, UNLESS OTHERWISE SPECIFIED:		DATA I/O	
DSN. ENGR.	DATE	MFG. ENGR.	DATE	QUAL. ASSUR.	DATE	TITLE SCHEMATIC DIAGRAM, POWER SUPPLY	
ENGR. MGR.	DATE	ENGR. MGR.	DATE	ENGR. MGR.	DATE		
DRAWN BY:		CHECKED BY:		DATE		SCALE NONE	
SIZE		CODE		D		54193	
D		30-702-1774		SHEET 1 OF 1			

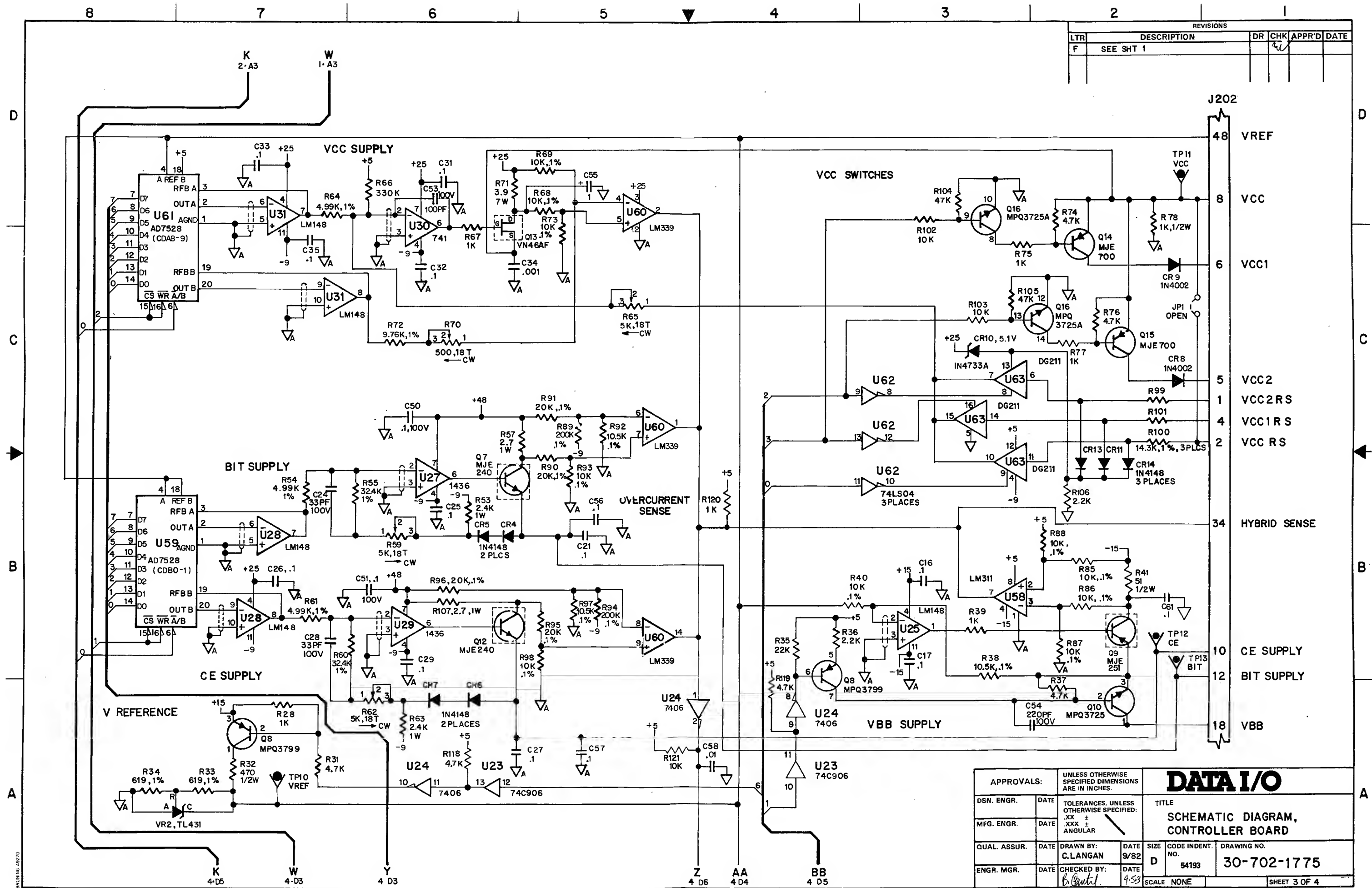


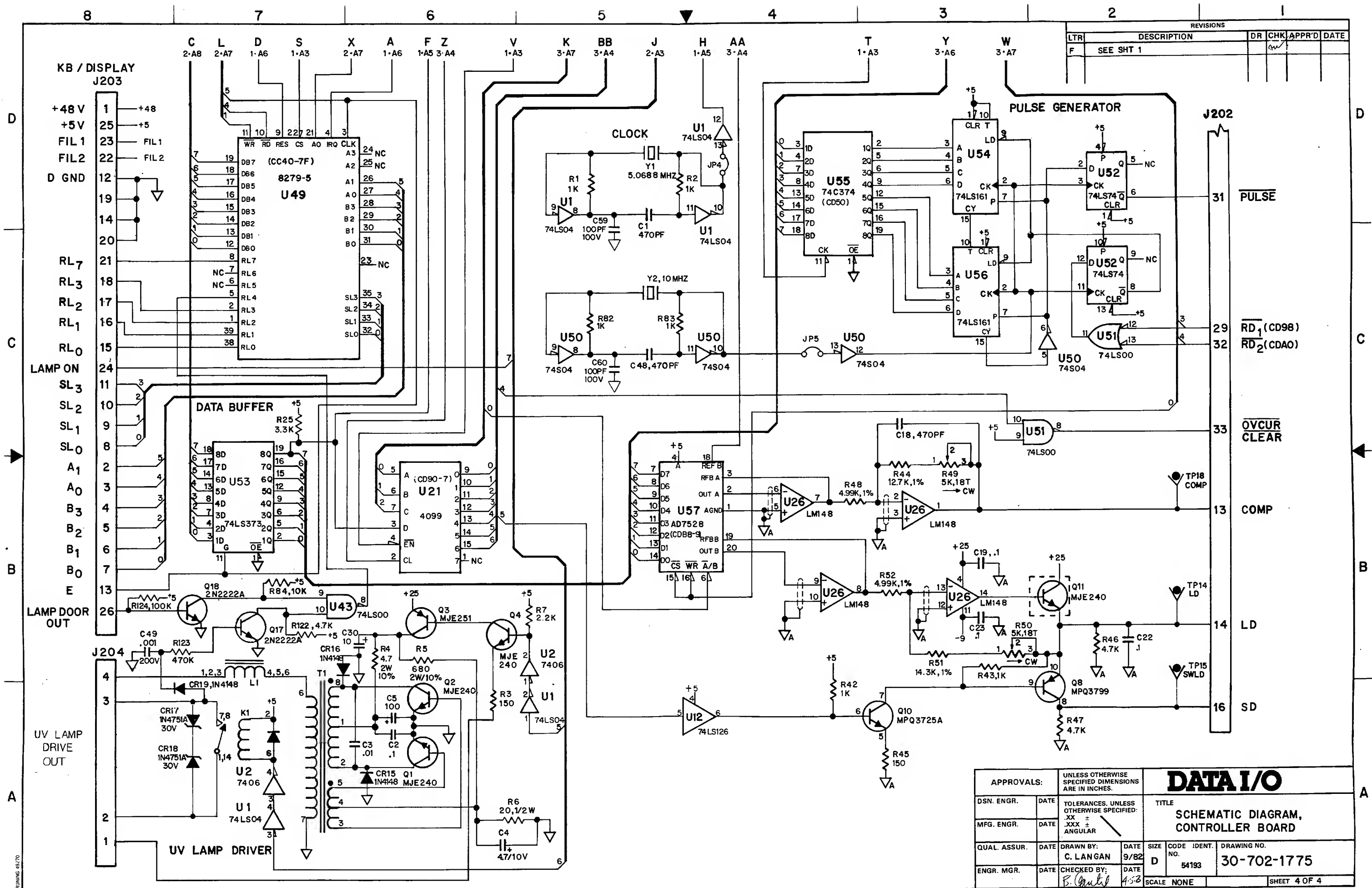


REVISIONS				
LTR	DESCRIPTION	DR	CHK	APPR'D DATE
F	SEE SHT 1			



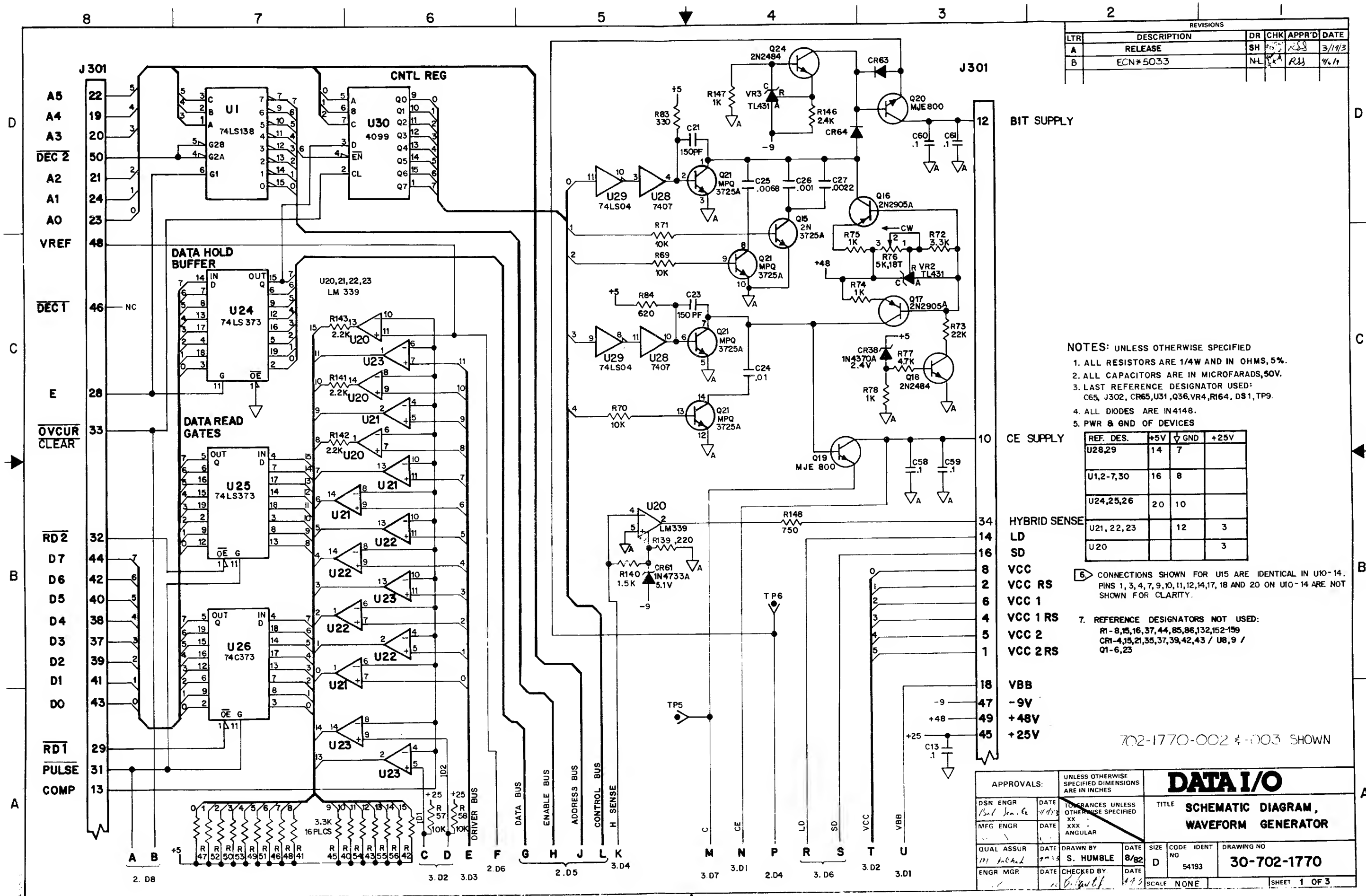
APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		TOLERANCES	
PROJ. ENGR.		DECIMALS	ANGULAR		
ENG. MGR.		.X ±	.XX ±		
		.XXX ±	.00 NOT SCALE DRAWING		
Q.C.		DRAWN BY:	M.P./C.L.		
DATE		CHECKED BY:	D. P. 4.5.3		
TITLE		SIZE	CODE	IDENT. NO.	DRAWING NO.
SCHEMATIC DIAGRAM, CONTROLLER BOARD		D		54193	30-702-1775
SCALE		NONE		SHEET 2 OF 4	

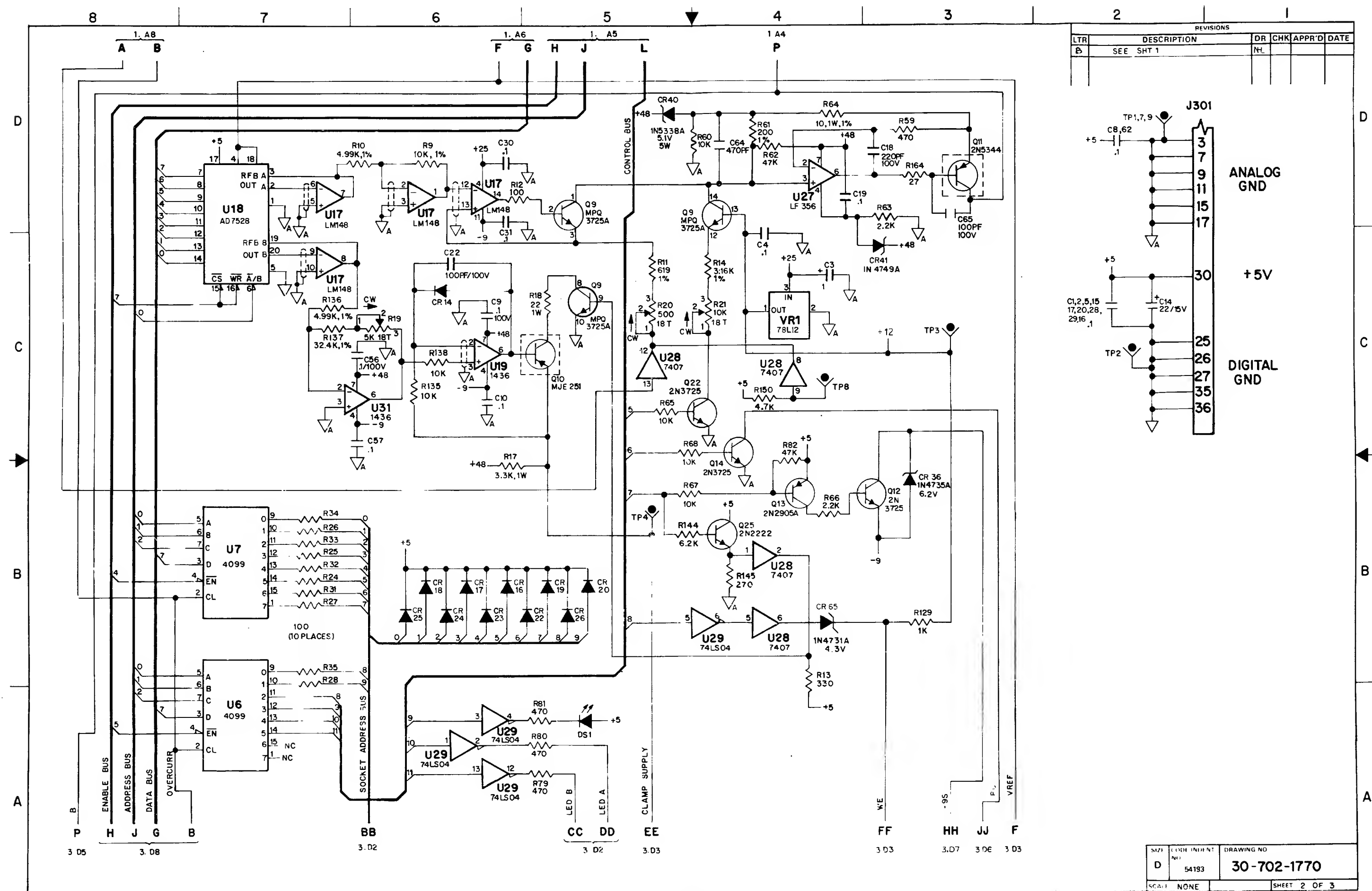












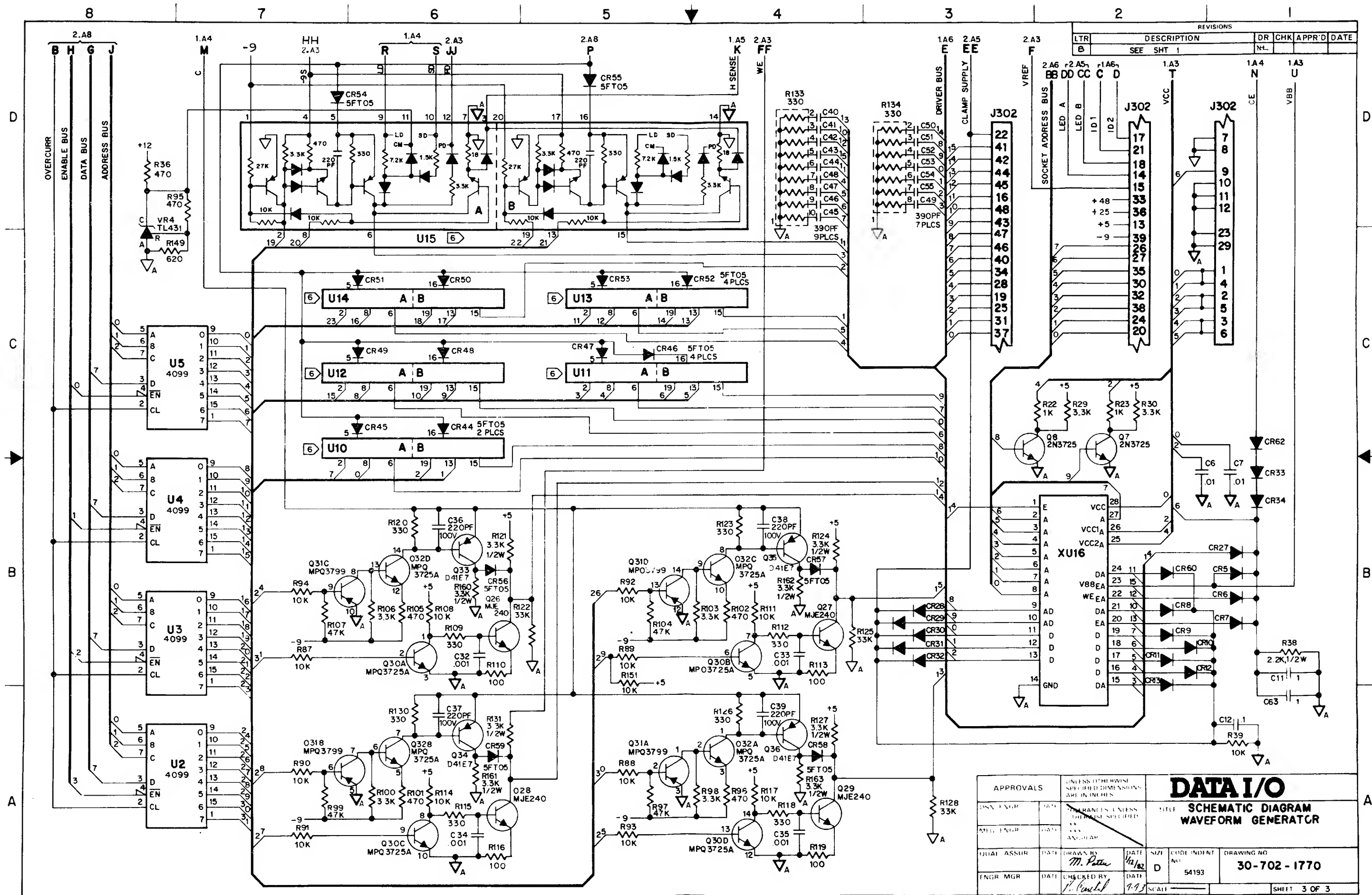


Figure 3-8. Verify Device

